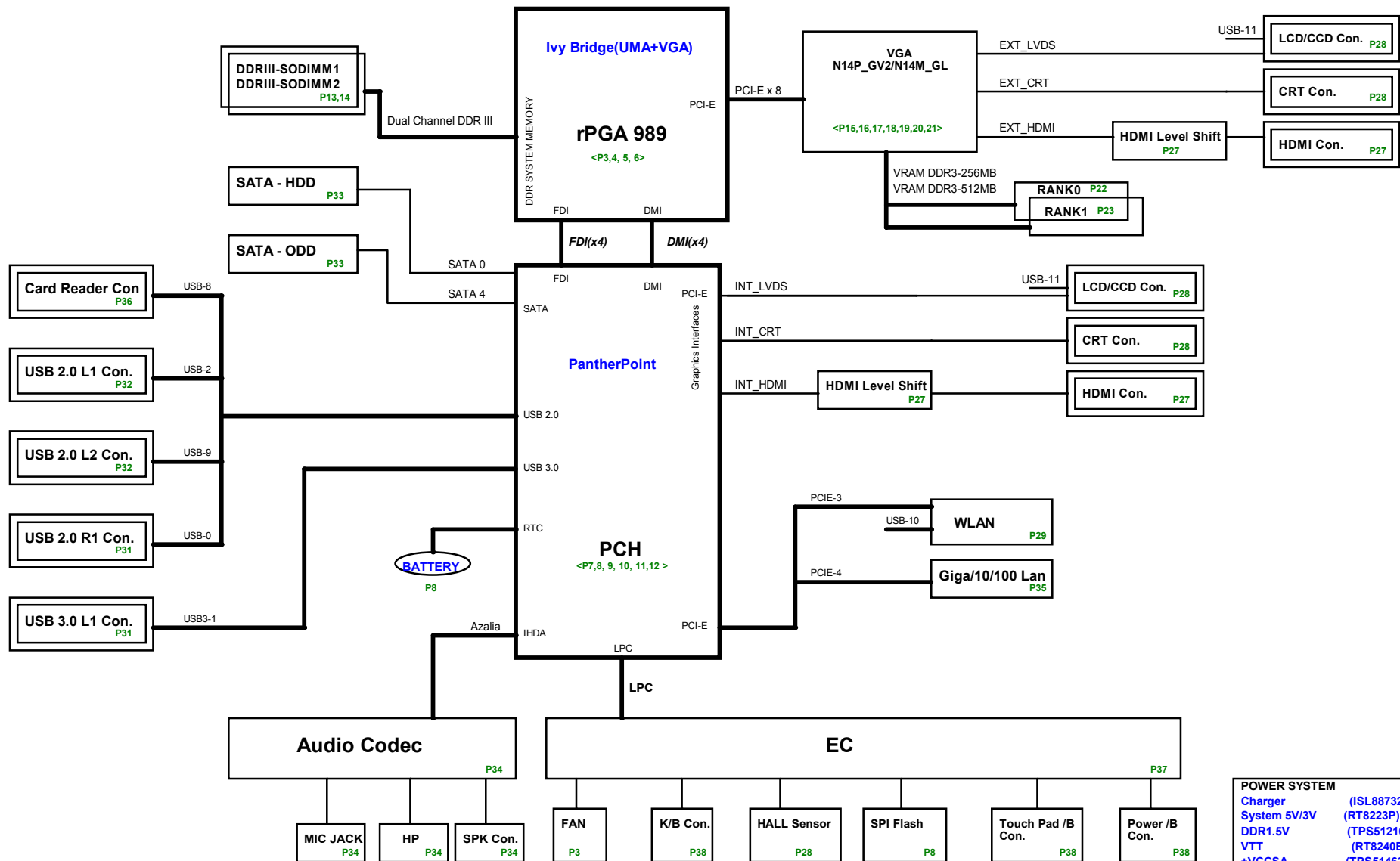
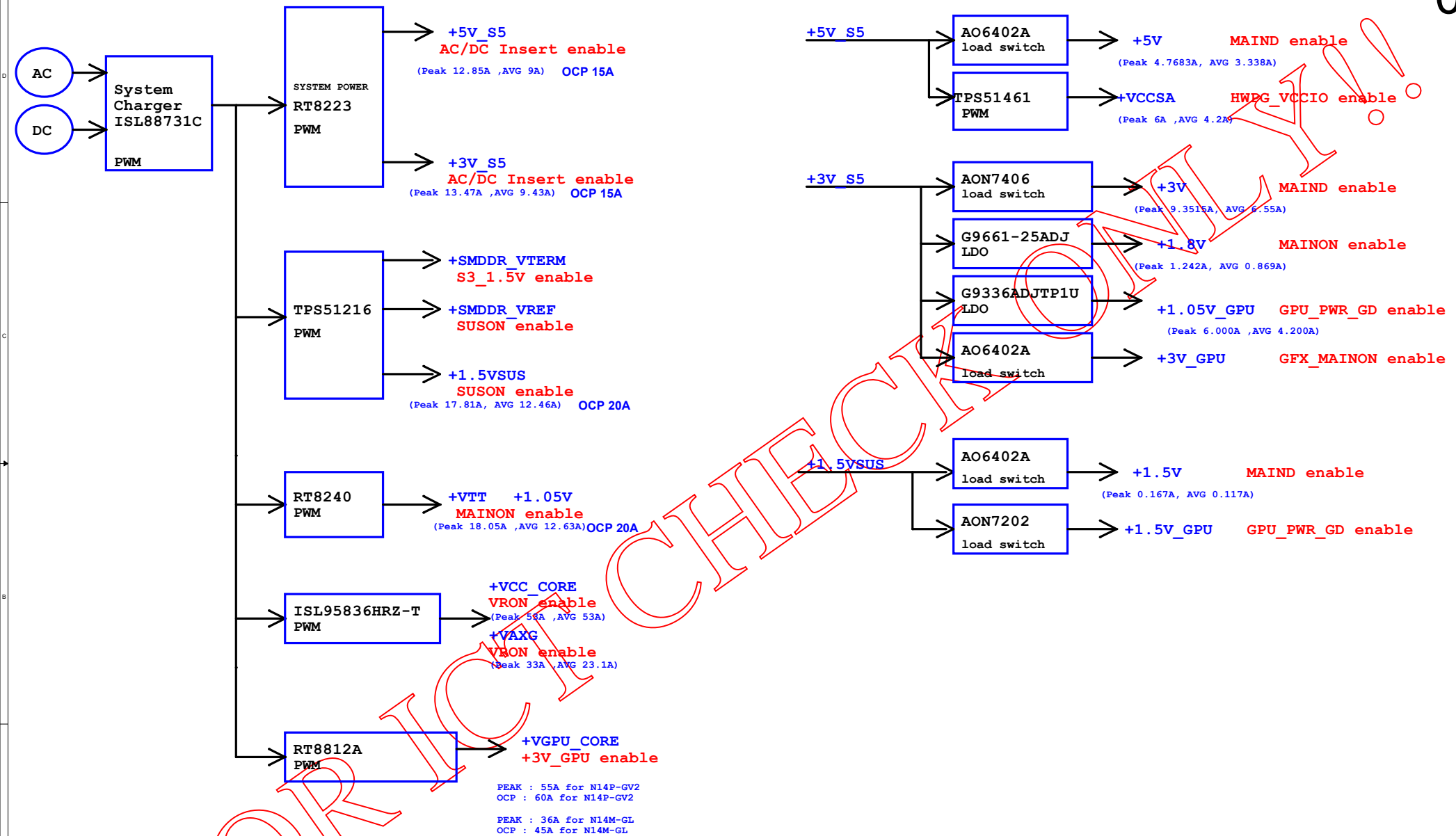


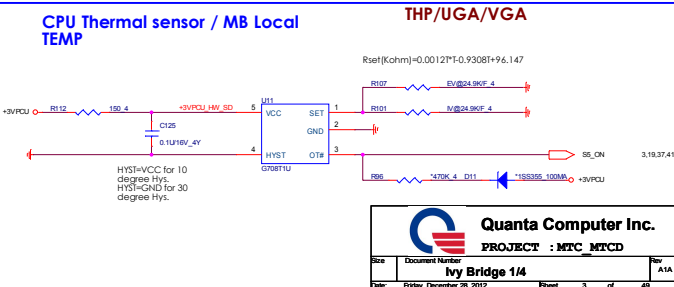
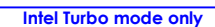
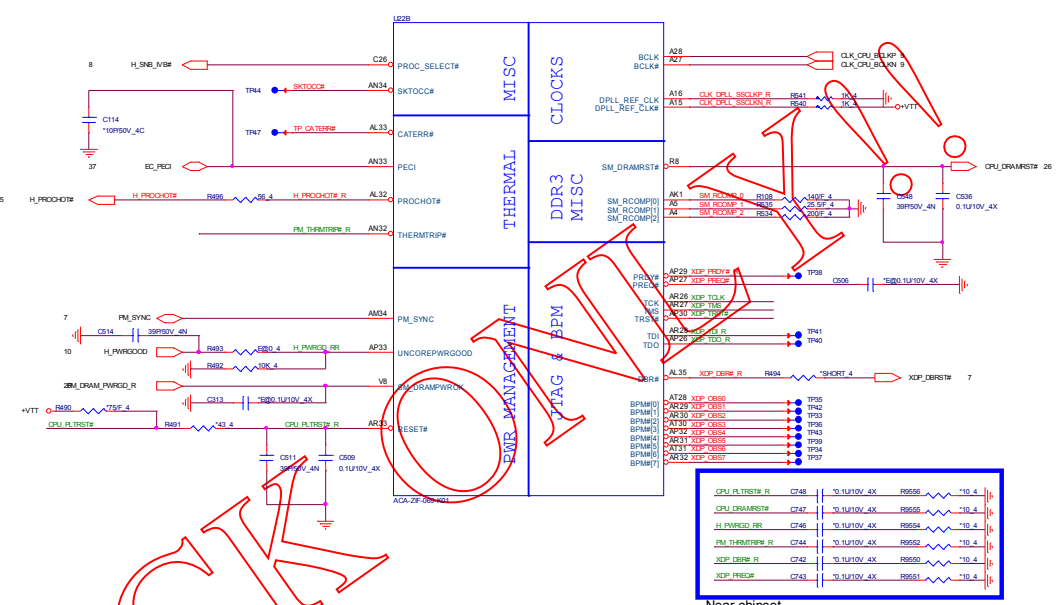
# Chief River Block Diagram

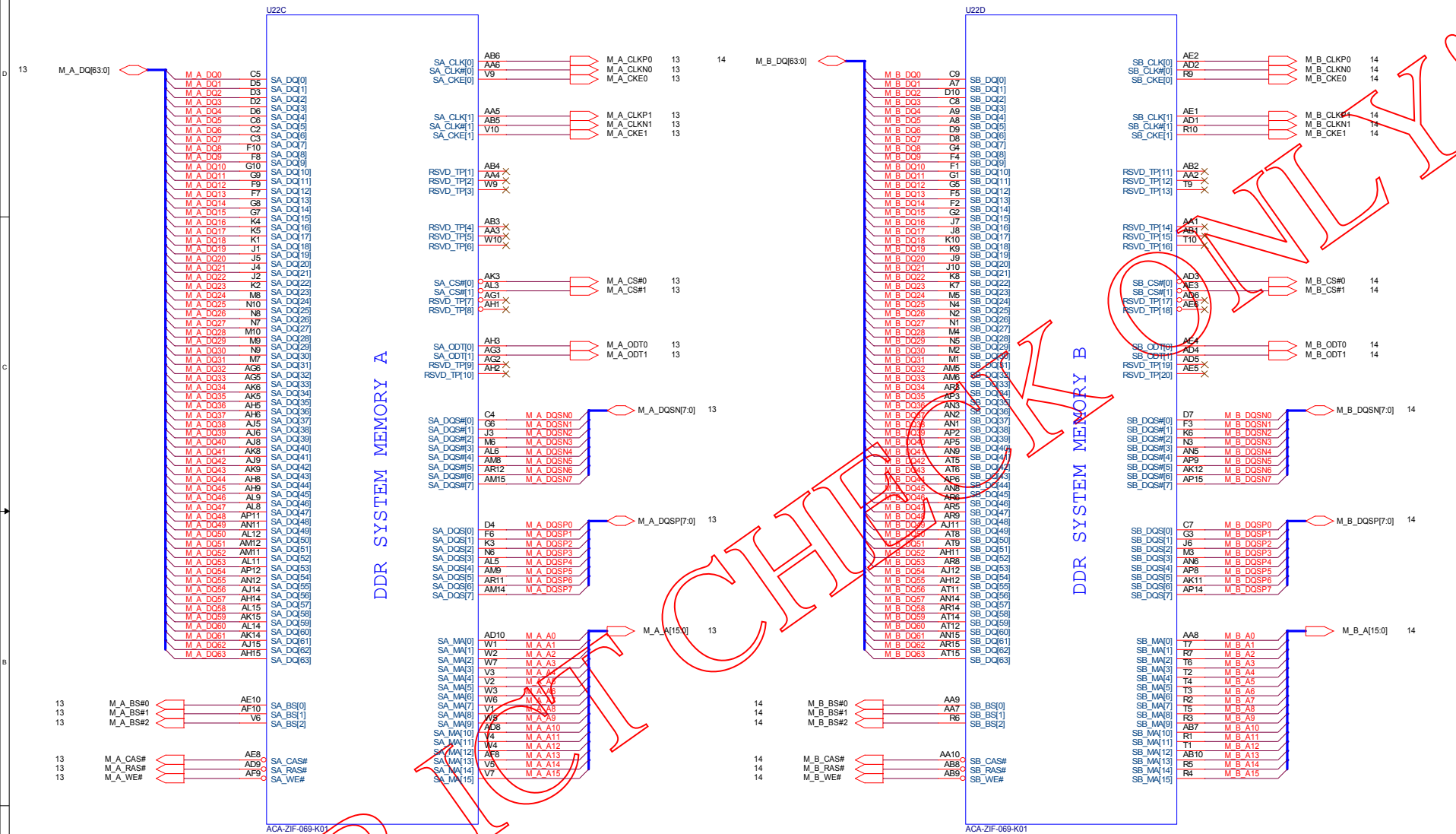
01

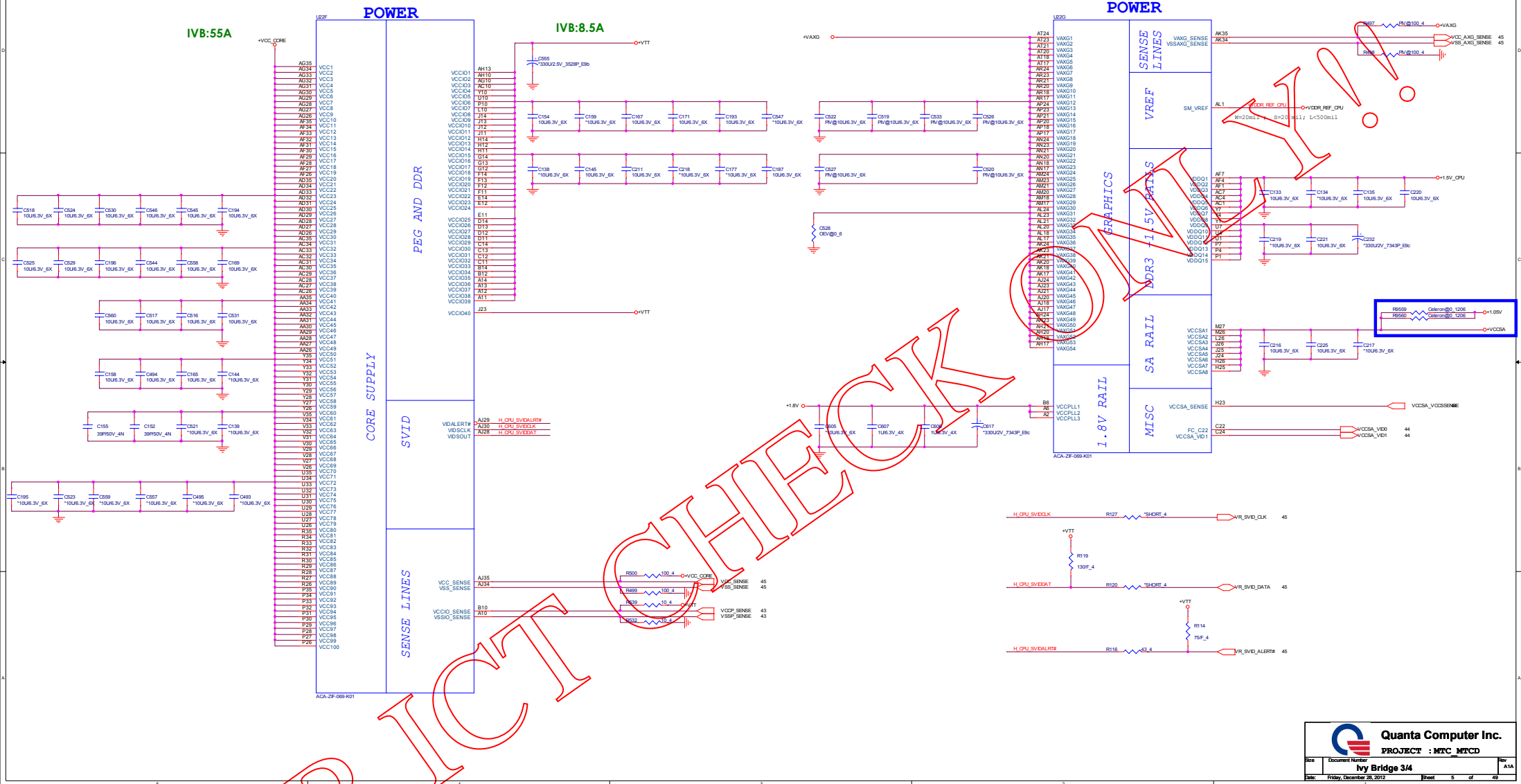


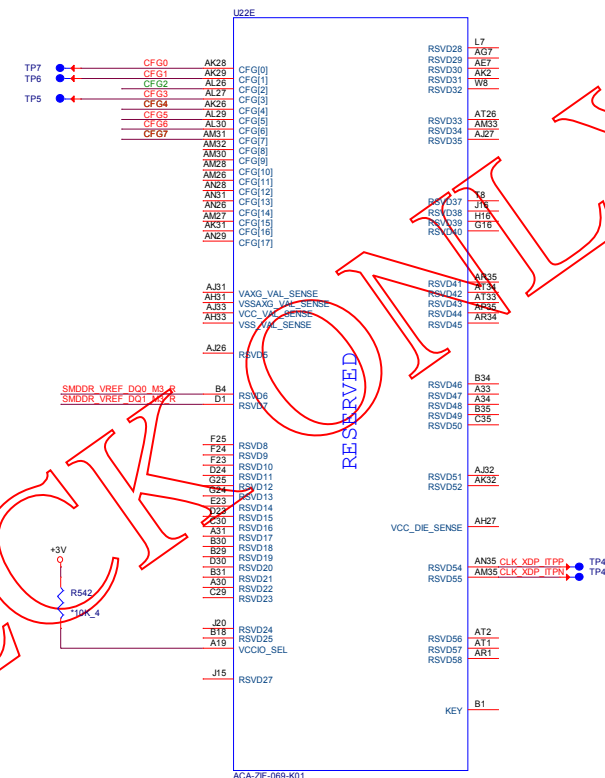
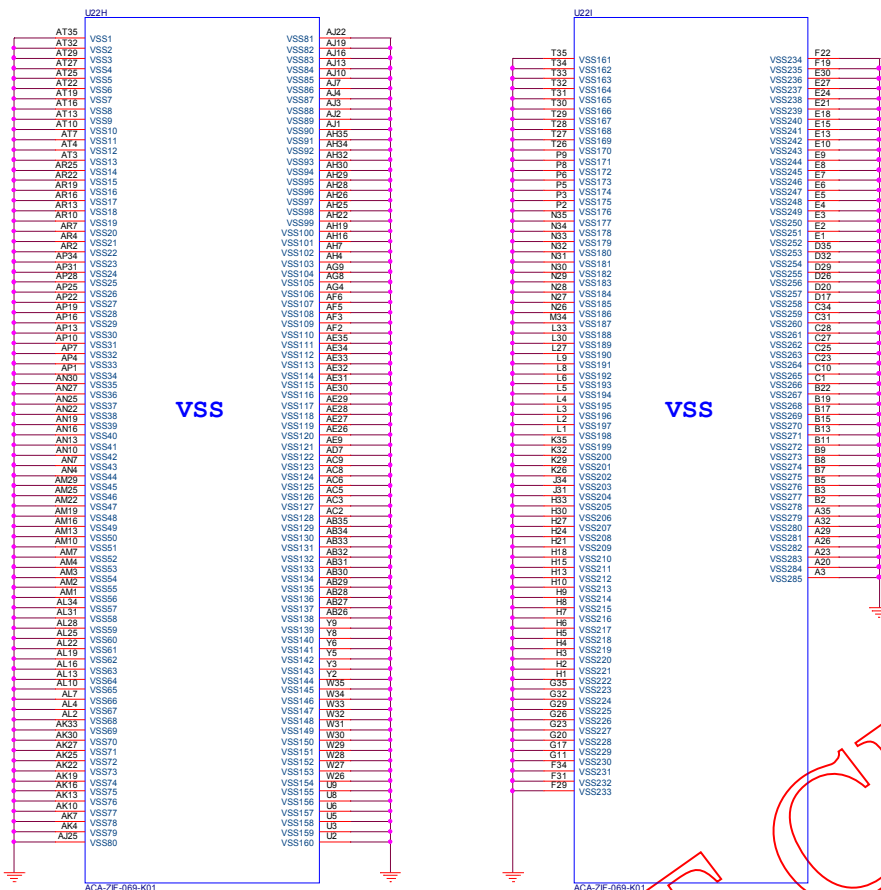
POWER SYSTEM		
Charger	(ISL88732HRTZ-T)	P40
System 5V/3V	(RT8223P)	P41
DDR1.5V	(TPS51216)	P42
VTT	(RT8240BGQW)	P43
+VCCSA	(TPS51462)	P44
+VCORE+VGFX	(ISL95836)	P45
+1.8V	(G966A)	P46
nVIDIA_GPU	(RT8812A)	P47









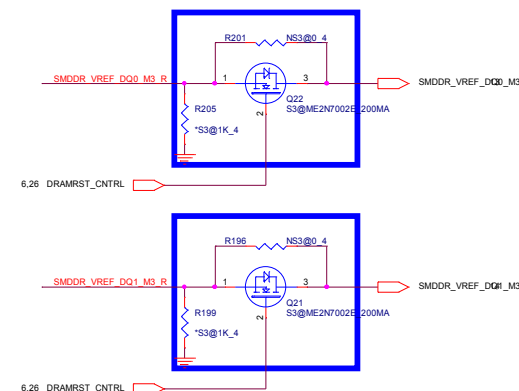


## Processor Strapping CPU/VGA

The CFG signals have a default value of "1" if not terminated on the board.

Pin Name	Configuration
CFG2 (PEG Static Lane Reversal -> 16 Lane)	1=Normal Operation 0=Lane Reversal
CFG3 (Reserved)	
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP
CFG5 CFG6 (PCIe Bifurcation)	00=x8.x4.x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable ; function 2 enable) 10=x8.x8 - Device 1 function 1 enable ; function 2 enable 11=(Default) x16 - Device 1 function 1 and 2 disable
CFG7 (PEG Defer Training)	1=PEG train immediately following xxRESETB de assertion 0=PEG wait for BIOS training

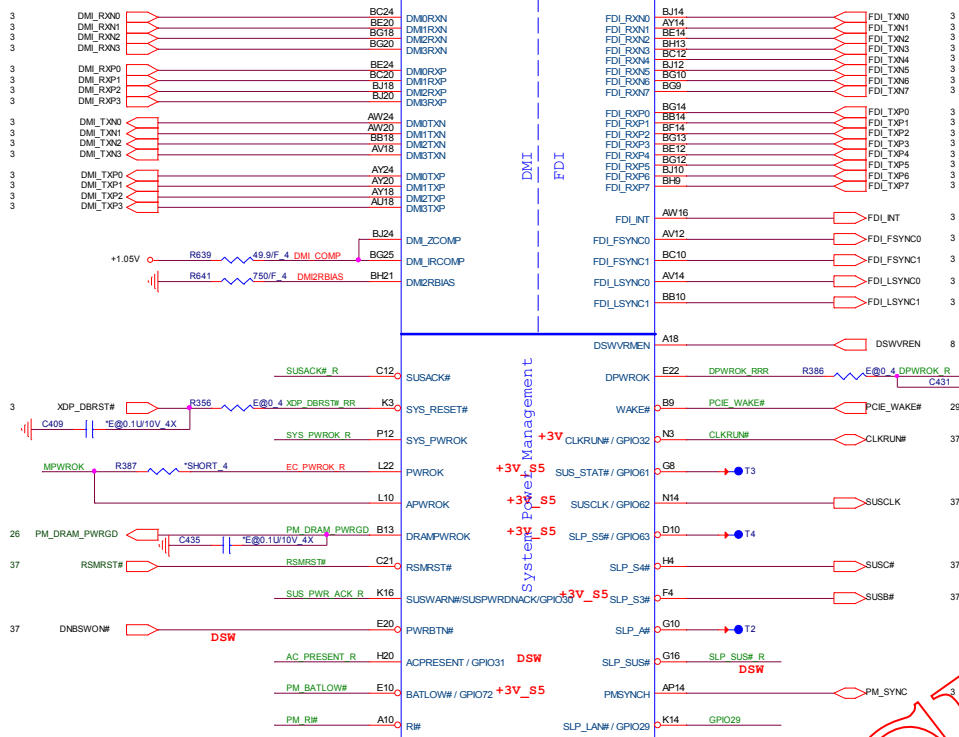
## DDR3 VREF DQ (M3) S3P





## Cougar Point (DMI, FDI, PM) CLG

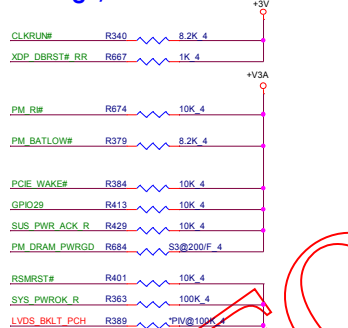
U26C



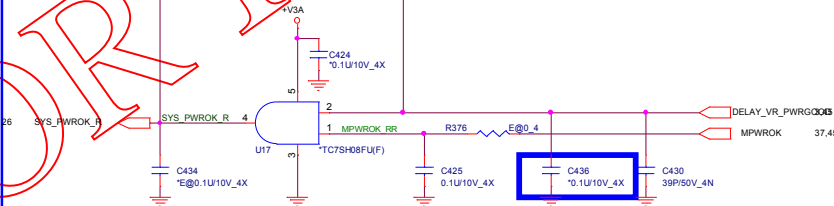
Near chipset



## PCH Pull-high/low

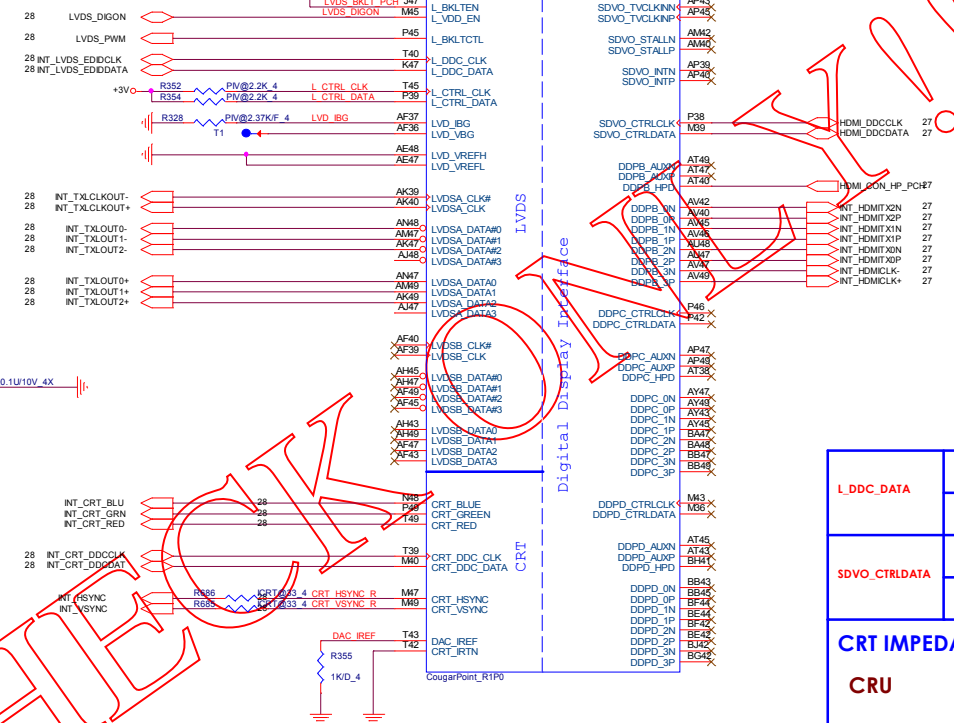


## System PWR OK

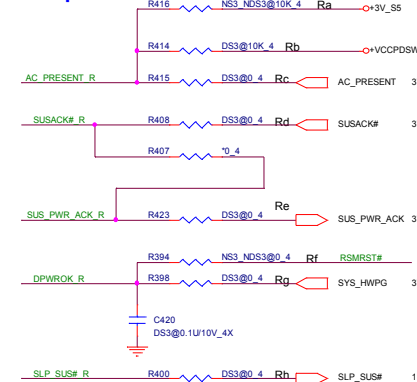


## Cougar Point (LVDS, DDI) CLG/CRU/LDU

U26D



## Deep Sx

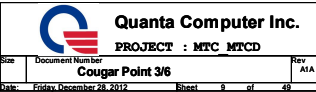


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb, Rc stuff	Ra stuff
SUS_PWR_ACK	Re stuff	Re stuff
SUSACK#_R	Rd stuff	Rf stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff





Cougar Point-M (PCI-E,SMBUS,CLK)CLG/GCK/MNG/U3C

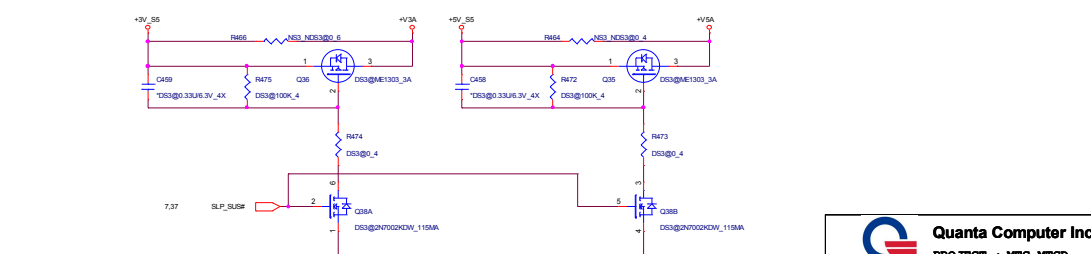
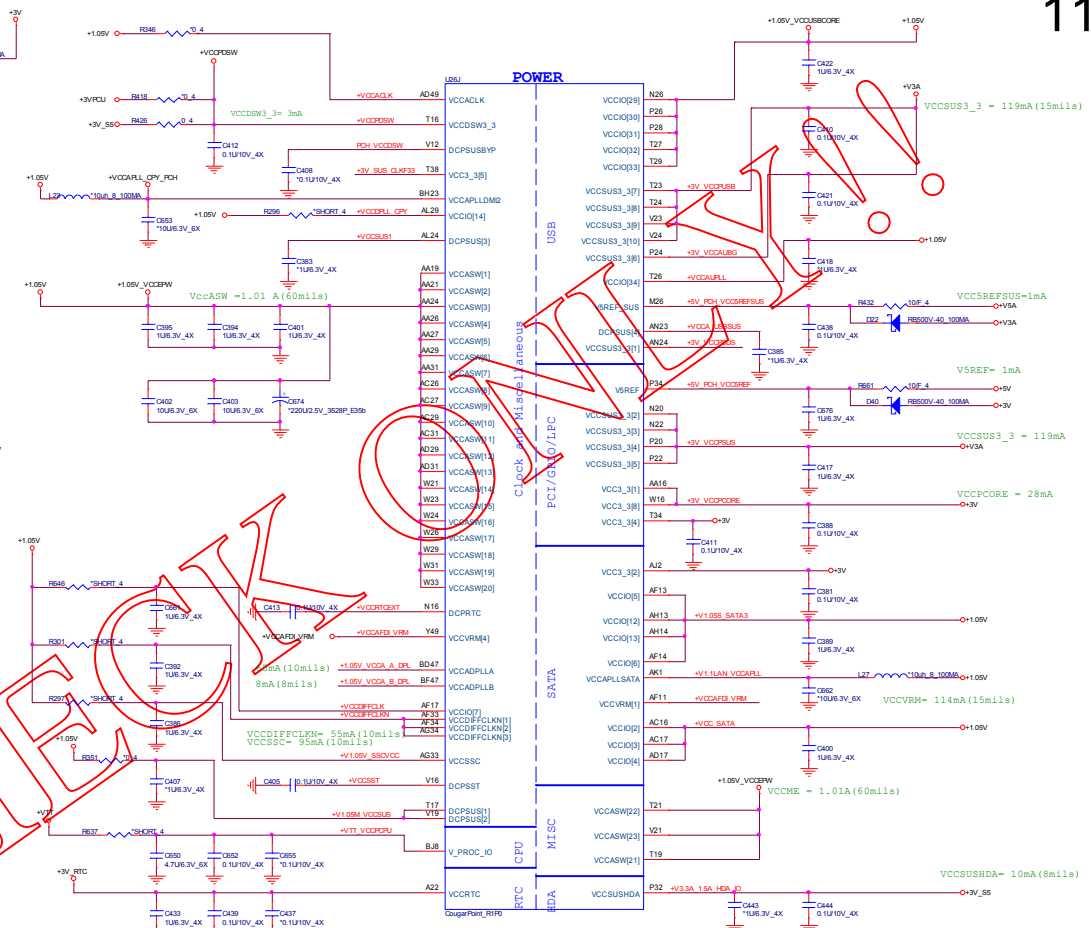




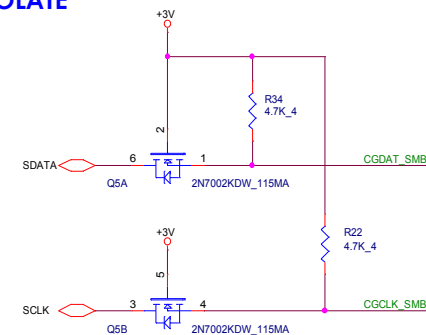
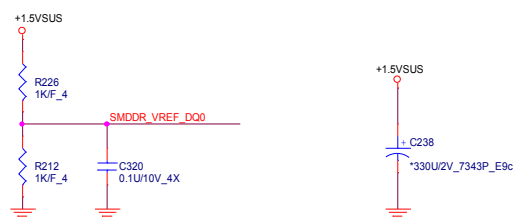
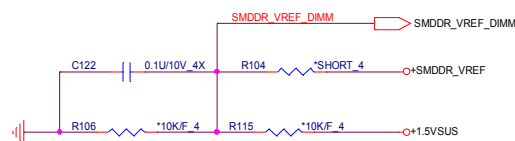
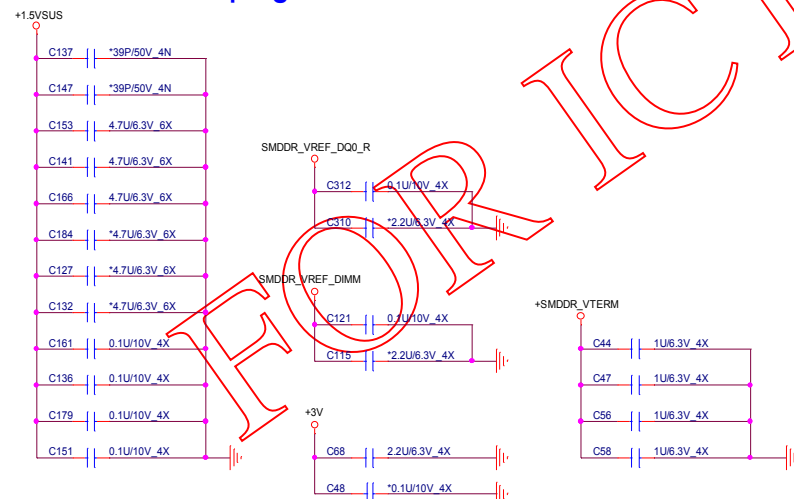
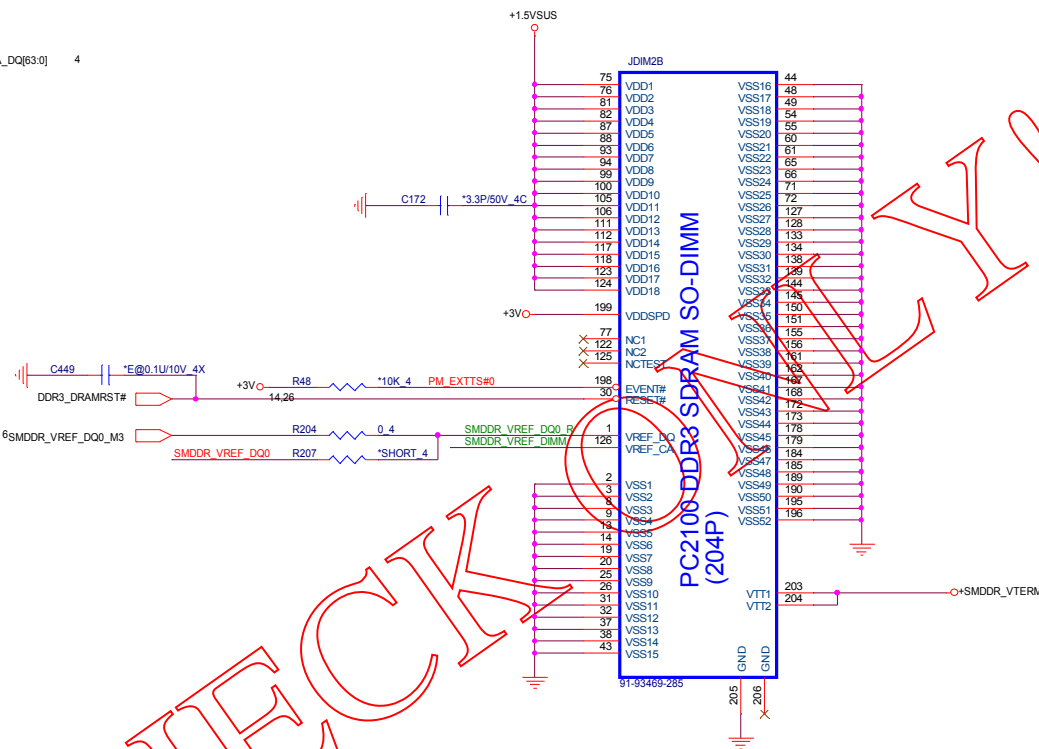
	Description	ID9	ID10	ID11
g	<u>U326/NSC6/UR6</u>	<u>L</u>	<u>L</u>	<u>L</u>
	ULU-2 and W/O USB Port	L	L	L
	<u>U336/NSC6/UR6</u>	<u>L</u>	<u>L</u>	<u>L</u>
	ULU-2 and W/O S&C UR-2	L	L	L
	<u>U36/NSC6/UR6</u>	<u>H</u>	<u>L</u>	<u>H</u>
	ULU-2 and W/O S&C UR-3	H	L	H
	<u>U326/SC6/UR6</u>	<u>L</u>	<u>H</u>	<u>H</u>
	ULU-2 and W/S&C UR-2	L	H	H
	<u>U36/SC6/UR6</u>	<u>H</u>	<u>H</u>	<u>H</u>
	ULU-2 and W/S&C UR-3	H	H	H

U3@	S&C@	UR@
NU3@	NS&C@	NUR@

ID_Detect	default
Metal/IMR	H
TEXTURE	L





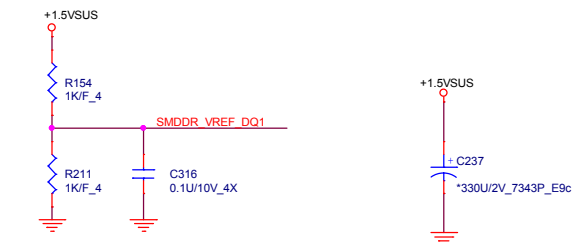




PC2100 DDR3 SDRAM SO-DIMM  
(204P)



DDR3 VREF DQ (M1)    **DDR**

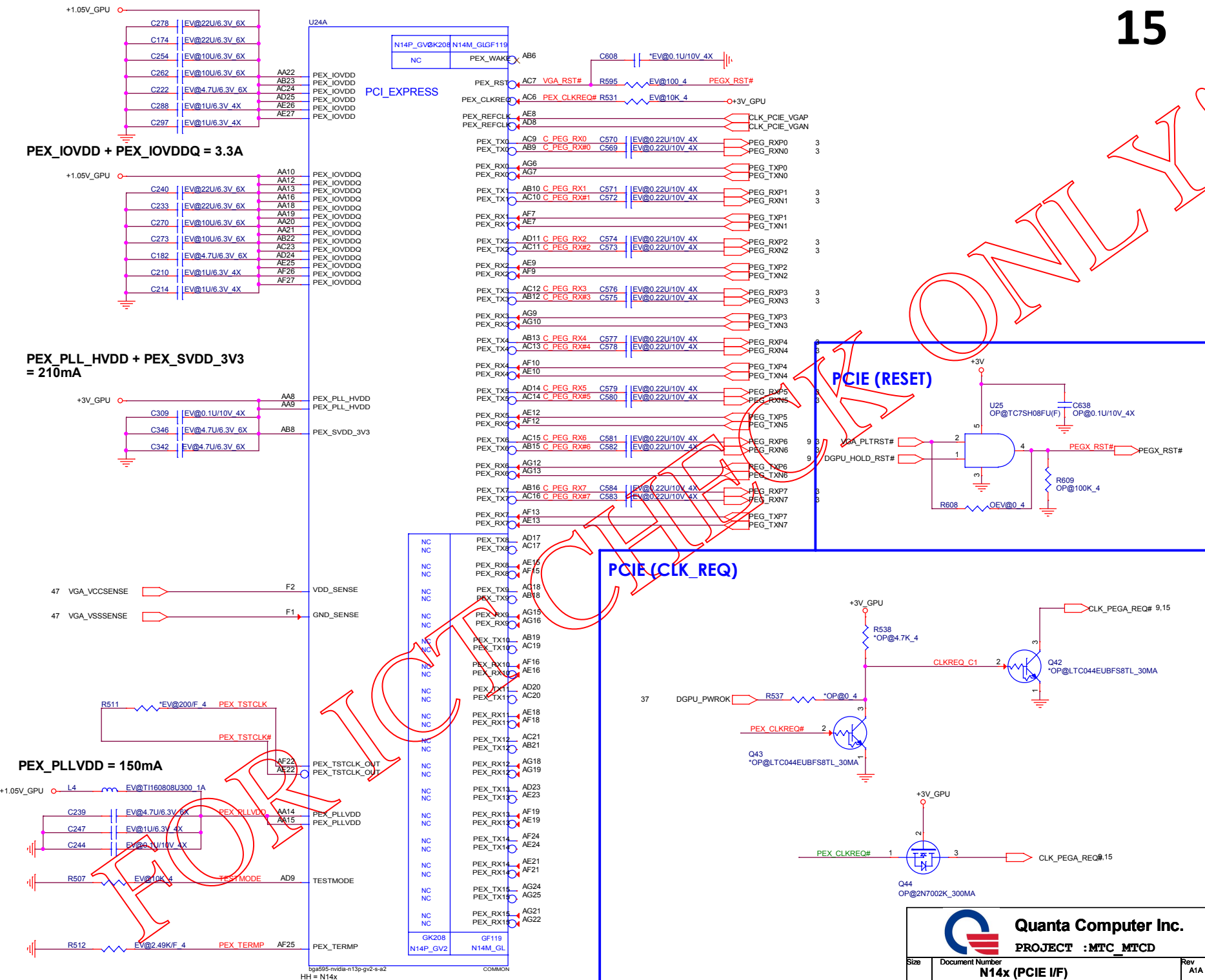




PEX\_IOVDD + PEX\_IOVDDQ = 3.3A

PEX\_PLL\_HVDD + PEX\_SVDD\_3V3 = 210mA

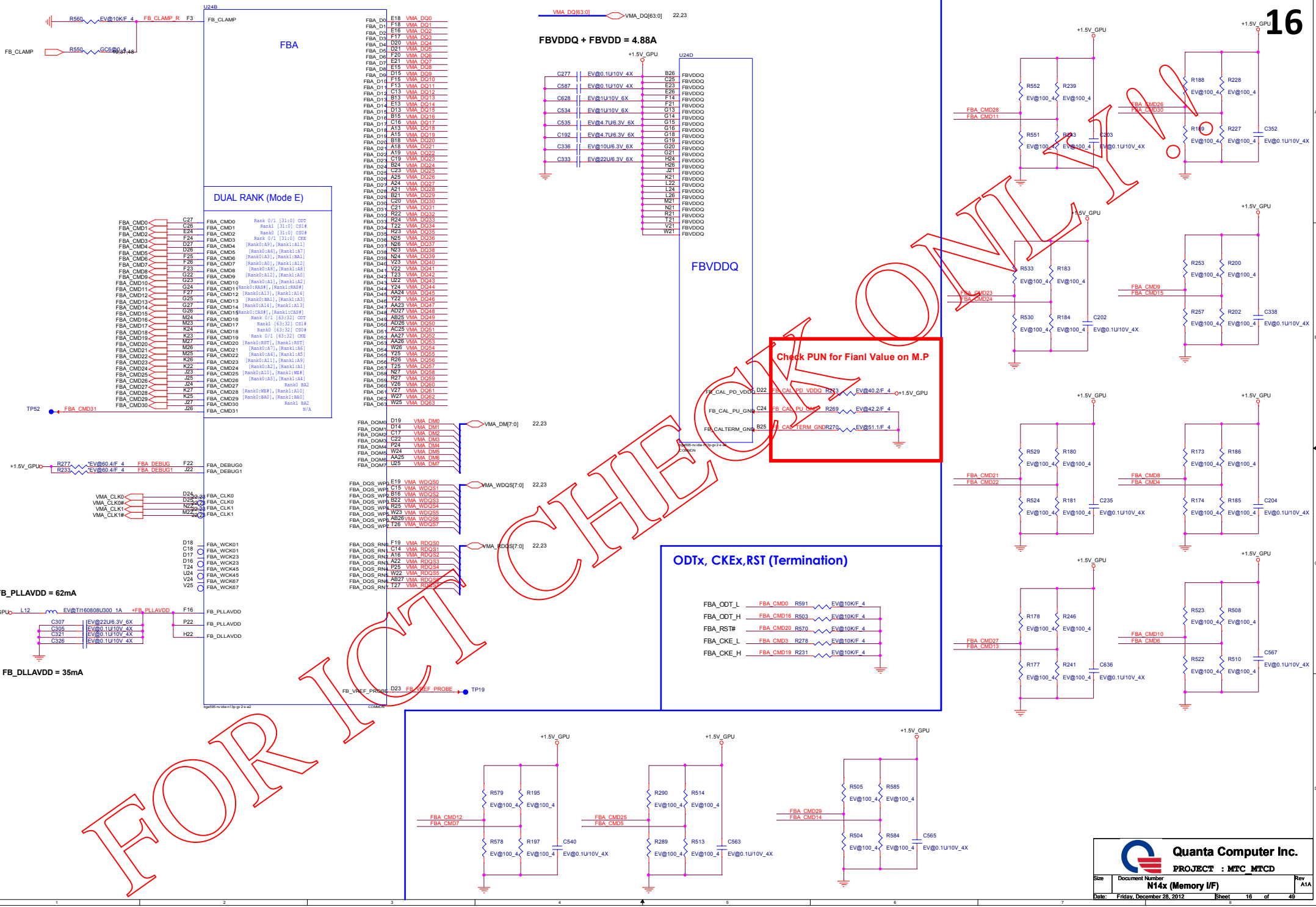
PEX\_PLLVDD = 150mA

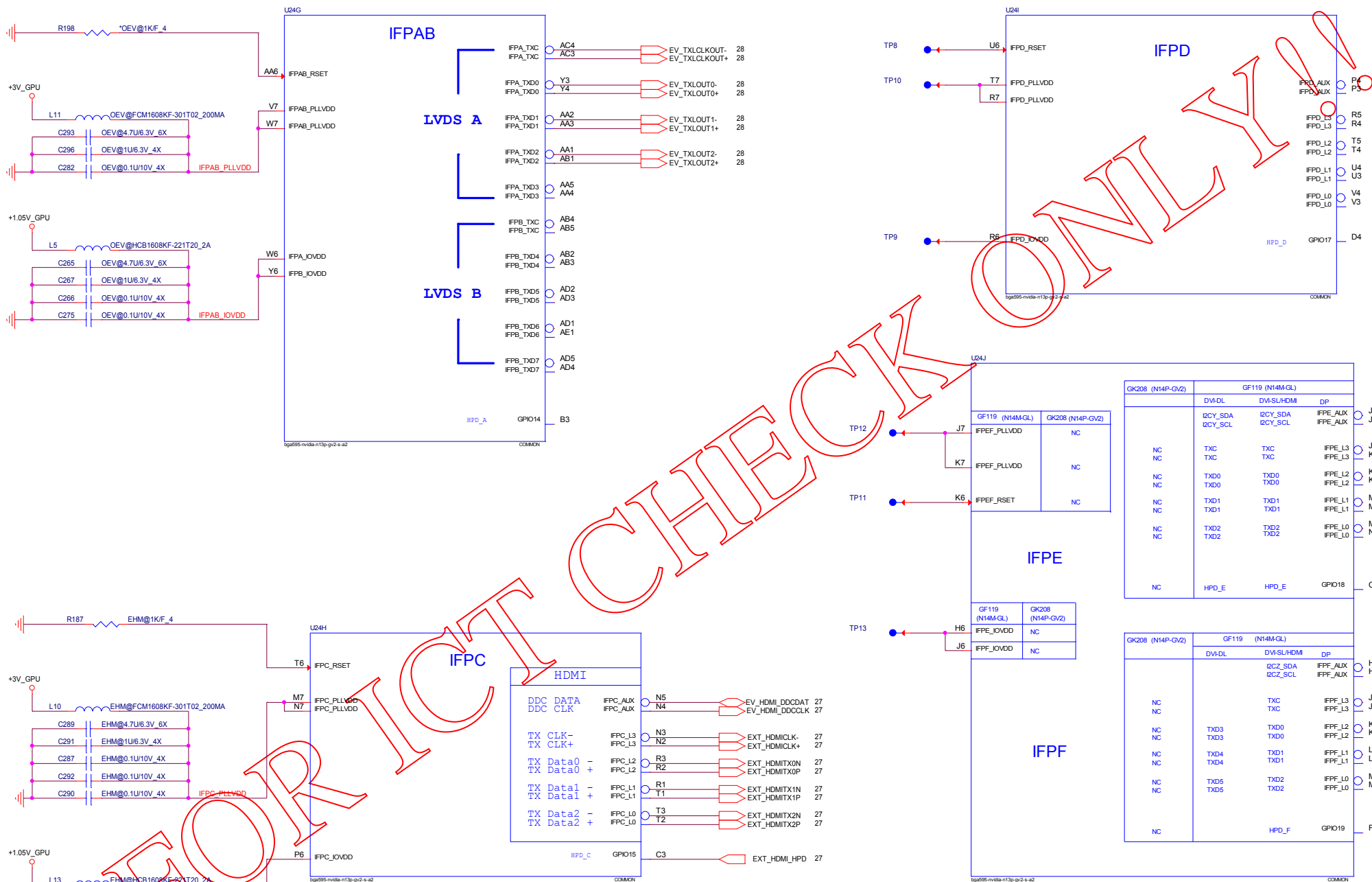


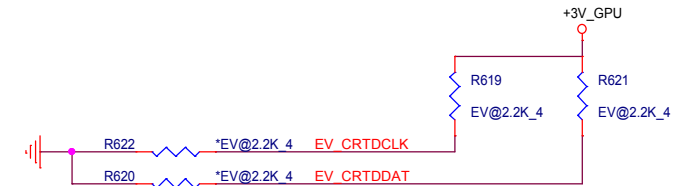
Quanta Computer Inc.


PROJECT : MTC\_MTCD

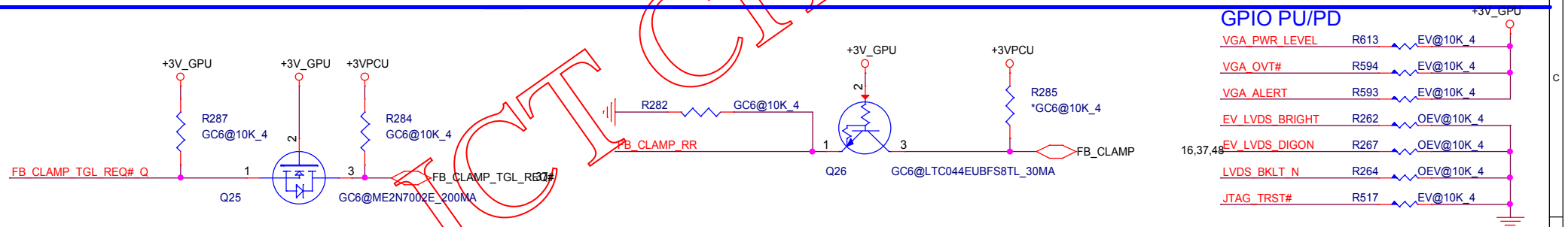
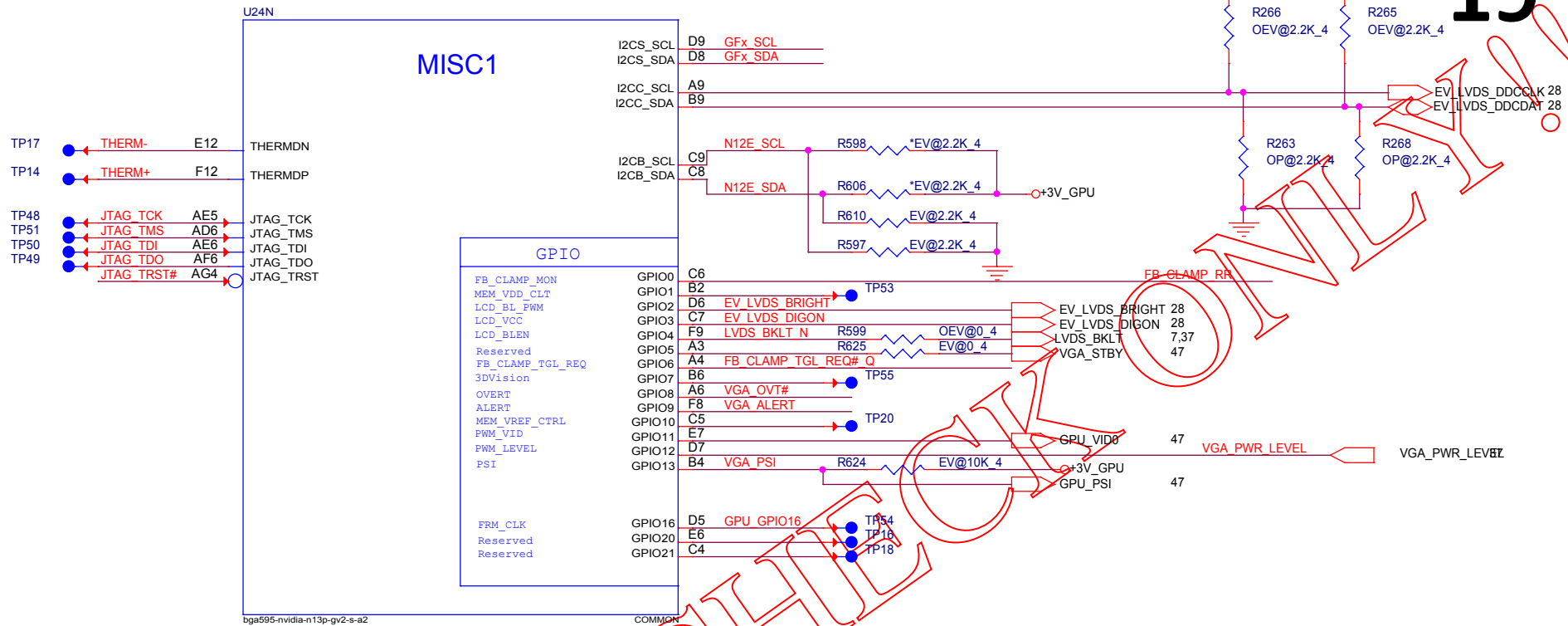
Size	Document Number	Rev
	N14x (PCIe I/F)	A1A
Date:	Friday, December 28, 2012	Sheet 15 of 49



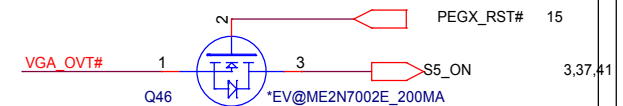
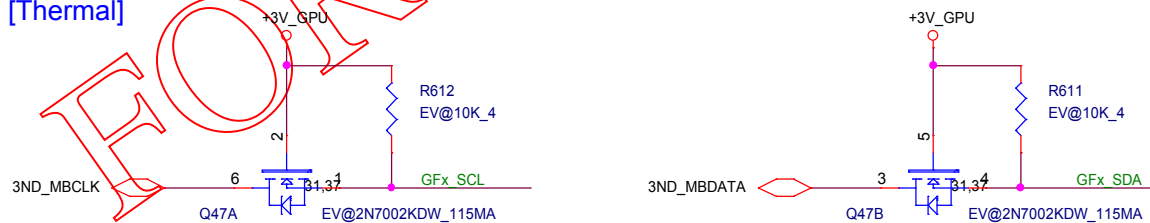


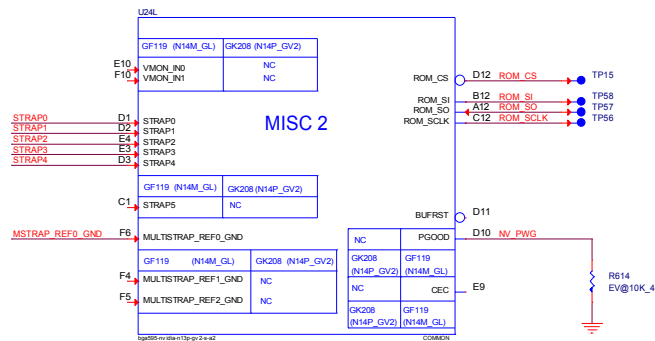


 <b>Quanta Computer Inc.</b> <b>PROJECT : MTC MTCB</b>			
Size	Document Number	Rev	
	<b>N14x (XTAL/CRT I/F)</b>	<b>A1A</b>	
Date:	Friday, December 28, 2012	Sheet	18 of 49



## SMBUS [Thermal]





	Vendor P/N	STN B/S P/N	Size	Strap		Note
128M	Hynix	H5TQ2G63DFR-N0C (128M*16) GL/GV2	128M=1GB	GL: 0x06	GV2: 0x06	
			128M=2GB		GV2: 0x06	
		H5TQ2G63DFR-11C (128M*16) GL/GV2	128M=1GB	GL: 0x06	GV2: 0x06	
			128M=2GB		GV2: 0x06	
	Samsung	K4W2G1646E-BC1A (128M*16) GL/GV2	128M=1GB	GL: 0x05	GV2: 0x07	
			128M=2GB		GV2: 0x07	
		K4W2G1646E-BC11 (128M*16) GL/GV2	128M=1GB	GL: 0x05	GV2: 0x07	
			128M=2GB		GV2: 0x07	
	Micron	MT41J128M16JT-107G:K (128M*16) GL/GV2	128M=1GB	GL: 0x01	GV2: 0x05	
			128M=2GB		GV2: 0x05	
256M	Micron	MT41K256M16HA-107G:E (256M*16) GL/GV2	256M=2GB	GL: 0x00	GV2: 0x01	
			256M=4GB		GV2: 0x01	
	Samsung	K4W4G1646B-HC11 (256M*16) GL/GV2	256M=2GB	GL: 0x0B	GV2: 0x03	
			256M=4GB		GV2: 0x03	
	Hynix	H5TQ4G63MFR-11C (256M*16) GL	256M=2GB	GL: 0x03		
			N/A			
			256M=2GB	GL: 0x04		
			N/A			

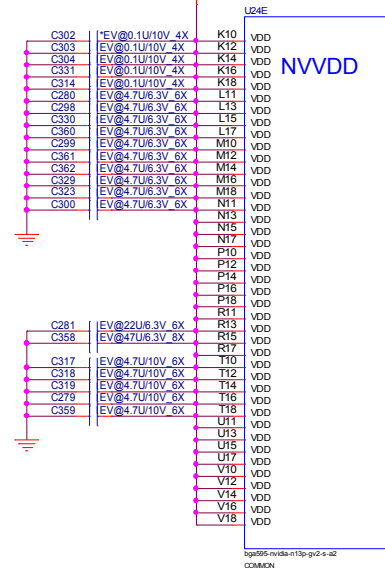
MULT STRIP [N14P_GV2]						
PCL_DEVID STRAP	PCI DEVICE ID	0x1292 -> QS 0x12AD -> ES	DP_PLL_VDD33	1 [Default]		
RAM_CFG	RAM_CFG[3:0] for memory configuration		PEX_PLL_EN_TERM	PCIe PLL termination 0:Disable [Default]; 1:Enable		
SUB_VENDOR	0:No VBIOS ROM; 1:BIOS ROM [Default]		3GIO_PADCFG	[0000] -> Gen3 support		
FB[1:0]	[1:0] -> 256MB		PCIE_MAX_SPEED	[1] -> Allow boot to PCIe Gen3		
VGA_DEVICE	0:3D Device; 1:VGA Device		PCIE_SPEED_CHANG_GEN3	[1] -> Enable Gen3		
SMB_ALT_ADDR [Slave address]	0:9E [Default]; 1:9C		SORx_EXPOSED	SOR0_EXP=0, SOR1_EXP=1 [IFPA/B.LVDS]; [IFPC/HDMI]		
USER STRAP	Panel EDID Support [0X1111]					
Strap Pin name	Strapping Bits 3	Strapping Bits 2	Strapping Bits 1	Strapping Bits 0	SETTING	NOTE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM	ROM_SCLK +3V_GPU - R626 -> V2@4.99K/F 4 - R612 -> V2@15K/F 4	
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI +3V_GPU - R630 -> V2@XXXX - R617 -> V2@XXXX	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	ROM_SO +3V_GPU - R548 -> V2@10K/F 4 - R616 -> V2@15K/F 4 +3V_GPU - R628 -> V2@4.99K/F 4	
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	STRAP0 +3V_GPU - R543 -> V2@45.3K/F 4 - R553 -> V2@15K/F 4	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	STRAP1 +3V_GPU - R605 -> V2@15K/F 4 - R566 -> V2@45.3K/F 4	
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	STRAP2 +3V_GPU - R549 -> V2@15K/F 4 - R558 -> V2@15K/F 4	
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	STRAP3 +3V_GPU - R545 -> V2_OEV@15K/F 4 - R555 -> V2_OEV@24.9K/F 4 +3V_GPU - R546 -> V2_OP@15K/F 4 - R556 -> V2_OP@4.99K/F 4	
STRAP4	RESERVED	PCIE_SPEED_CHAN CE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	STRAP4 +3V_GPU - R580 -> V2@15K/F 4 - R571 -> V2@45.3K/F 4	
4.99K	1000	0000	24.9K	1100	0100	
10K	1001	0001	30.1K	1101	0101	
15K	1010	0010	34.8K	1110	0110	
20K	1011	0011	45.3K	1111	0111	
Resistor Value	VDD33	GND	Resistor Value	VDD33	GND	
					MSTRAP_REF0_GND - R272 -> V2@40.2K/F 4	

Binary Strap [N14M_GL]				
Strap Pin name	Strap Mapping	Polarity	SETTING	
ROM_SCLK	SMB_ALT_ADDR	Pull-down to GND	+3V_GPU - R615 -> GL@10K/F 4 - R603 -> GL@10K 4	
ROM_SI	SUB_VENDER	Pull-Up to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM	ROM_SI +3V_GPU - R529 -> GL@10K/F 4 - R605 -> GL@10K 4	
ROM_SO	VGA_DEVICE	Pull-down to GND ( no dispaly )	ROM_SO +3V_GPU - R627 -> GL@10K/F 4 - R604 -> GL@10K 4	
STRAP0	RAMCFG[0]	USER defined	STRAP0 +3V_GPU - R544 -> GL@XXXX - R554 -> GL@XXXX	
STRAP1	RAMCFG[1]	USER defined	STRAP1 +3V_GPU - R568 -> GL@XXXX - R569 -> GL@XXXX	
STRAP2	RAMCFG[2]	USER defined	STRAP2 +3V_GPU - R548 -> GL@XXXX - R559 -> GL@XXXX	
STRAP3	RAMCFG[3]	USER defined	STRAP3 +3V_GPU - R547 -> GL@XXXX - R557 -> GL@XXXX	
STRAP4	PCIE_MAX_SPEED	Pull-down to GND	STRAP4 R581 -> GL@10K 4	

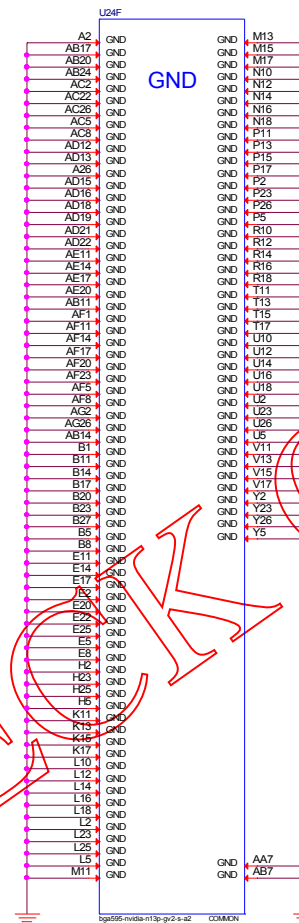
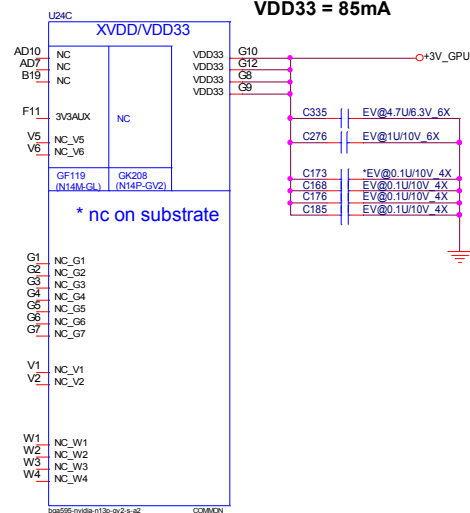


NVDD = 32.22 ~ 26.66 A

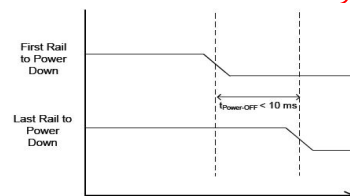
+VGPU\_CORE



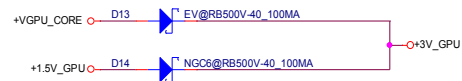
VDD33 = 85mA



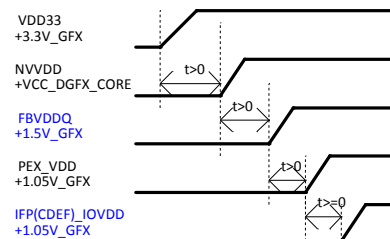
## Power down sequence



for meet Power down sequence for +3V\_GFX



## Power up sequence



Quanta Computer Inc.

PROJECT : MTC\_MTC

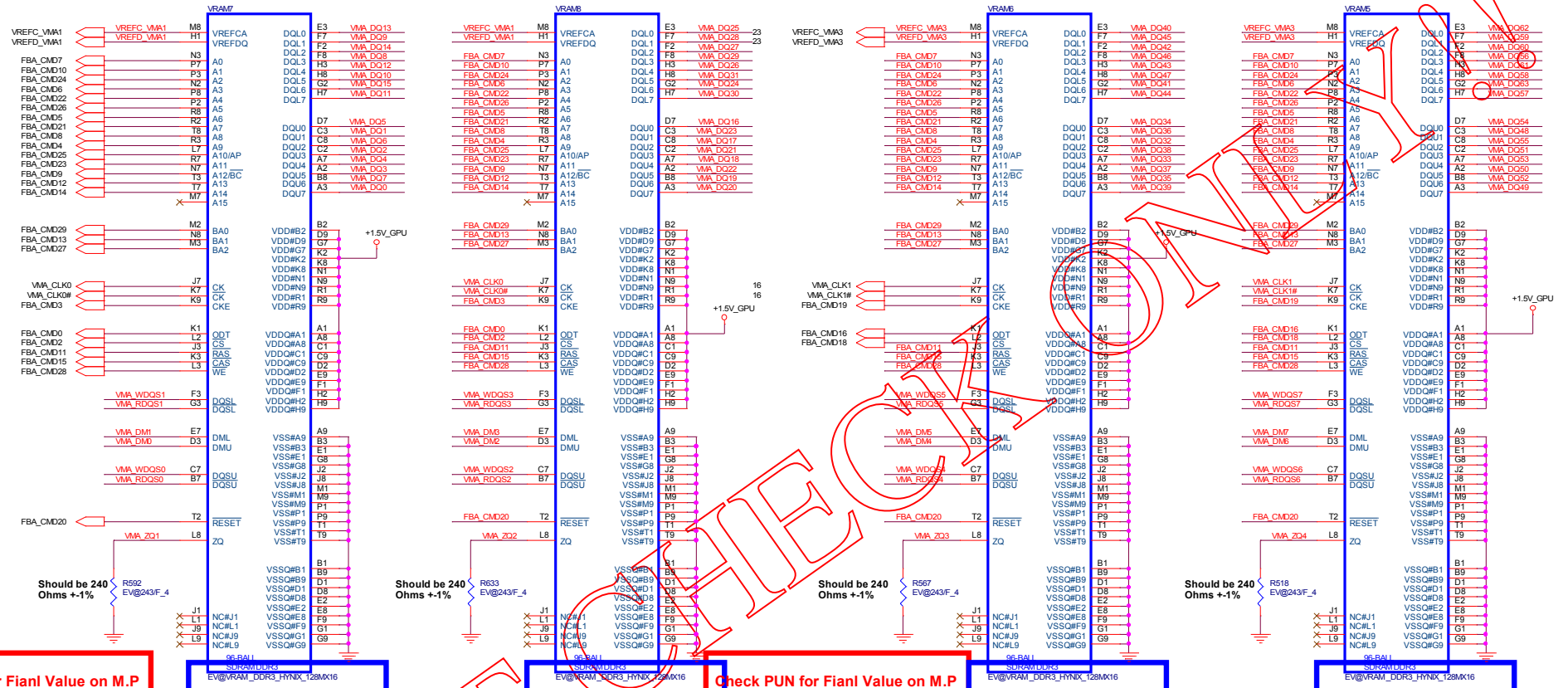
Size	Document Number	Rev
	<b>N14x (Power/GND)</b>	A1A
Date:	Friday, December 28, 2012	Sheet 21 of 49

## RANK0: 256MB/512MB DDR3

DataBus [0:31]

DataBus [64:32]

16.23 VMA\_DQ[63:0]  
16.23 VMA\_DM[7:0]  
16.23 VMA\_WDQS[7:0]  
16.23 VMA\_RDQS[7:0]



Check PUN for Fianl Value on M.P

Check PUN for Fianl Value on M.P

CLK-A0 Termination

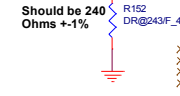
MEM Reference Voltage (Low)

CLK-A1 Termination

MEM Reference Voltage (High Bus)

VRAM De-Coupling

– DataBus [64:32]



Two circuit diagrams illustrating the connection of the +1.5V\_GPU supply to various components. Each component is connected to a 1.5V supply and a 10uF/0.4V capacitor.

**Left Diagram (+1.5V\_GPU):**

- C242: DR@1U6.3V\_4X
- C274: DR@1U6.3V\_4X
- C249: DR@1U6.3V\_4X
- C327: DR@1U6.3V\_4X
- C589: DR@0.1U10V\_4X
- C635: DR@0.1U10V\_4X

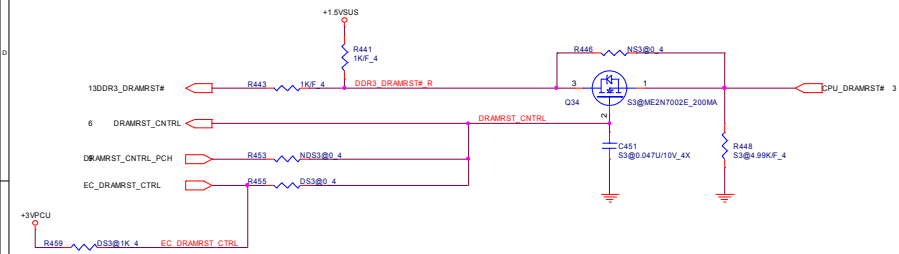
**Right Diagram (+1.5V\_GPU):**

- C199: DR@1U6.3V\_4X
- C206: DR@1U6.3V\_4X
- C255: DR@1U6.3V\_4X
- C256: DR@1U6.3V\_4X
- C837: DR@0.1U10V\_4X
- C590: DR@0.1U10V\_4X

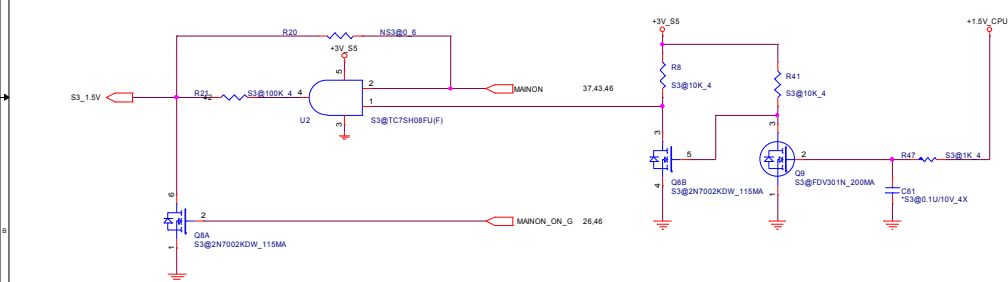


FOR ICT CHECK ONLY!!

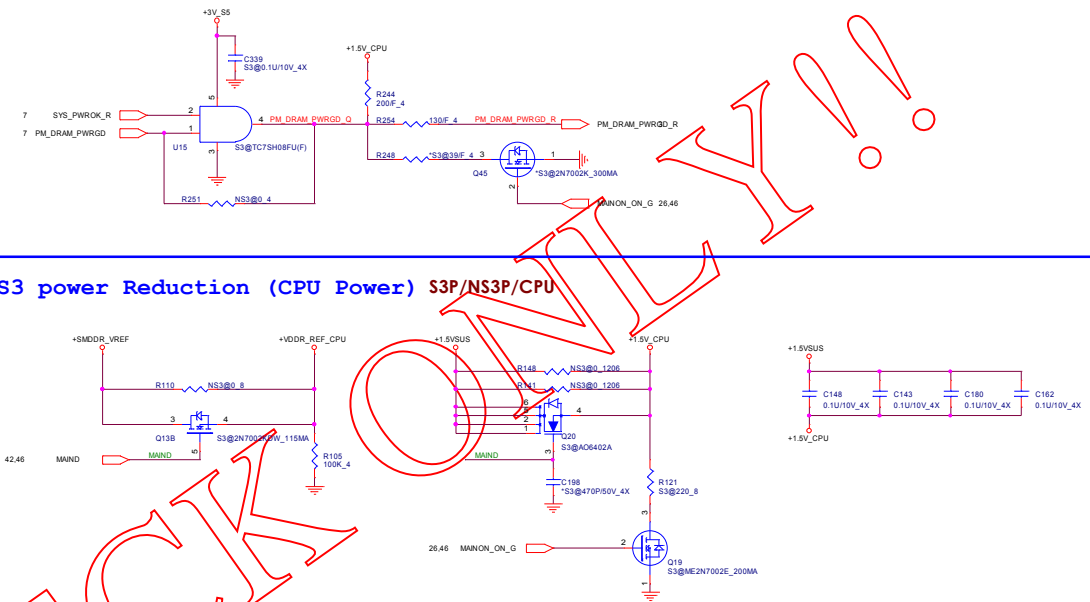
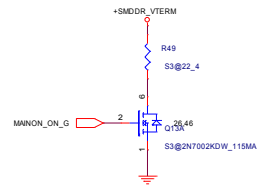
FOR ICT CHECK ONLY!!



For S3 power Reduction Sequence **S3P/NS3P/CPU**

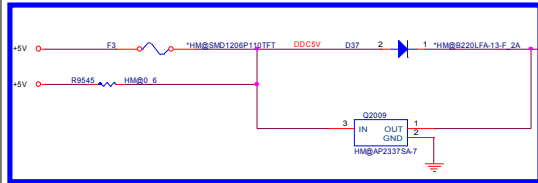
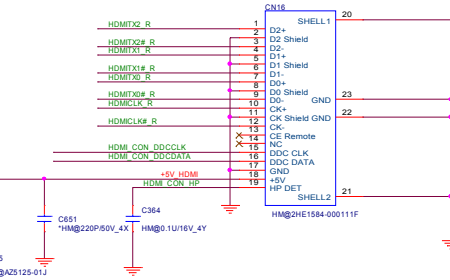
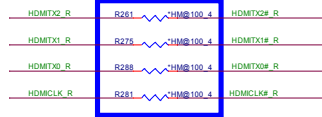
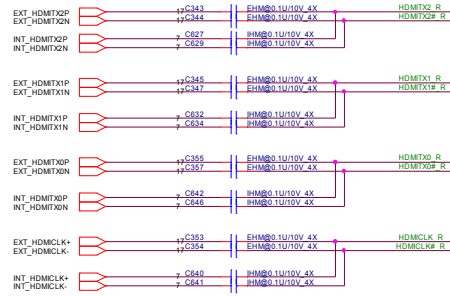


For S3 power Reduction VTT discharge S3P/NS3P/CPU

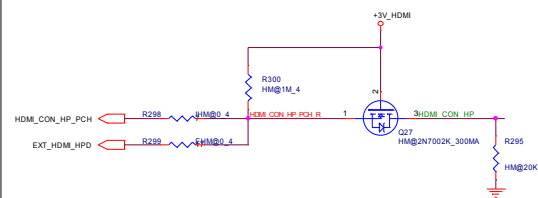




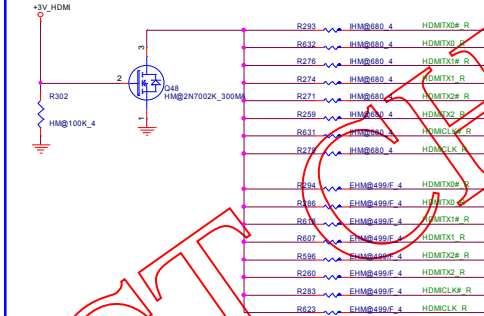
## HDMI Conn HDM/HMU/HMV



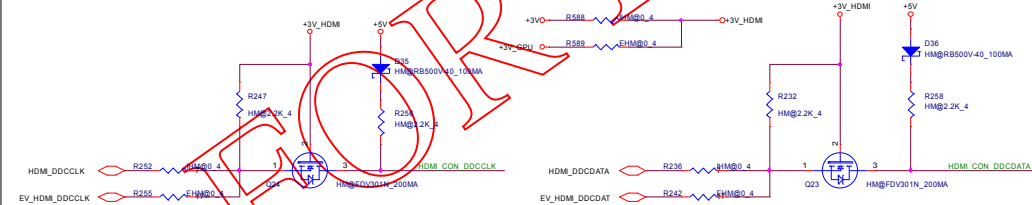
## HDMI-HPD HDM/HMU/HMV

HDMI  
LEVEL  
SHIFT

## HDM/HMU/HMV



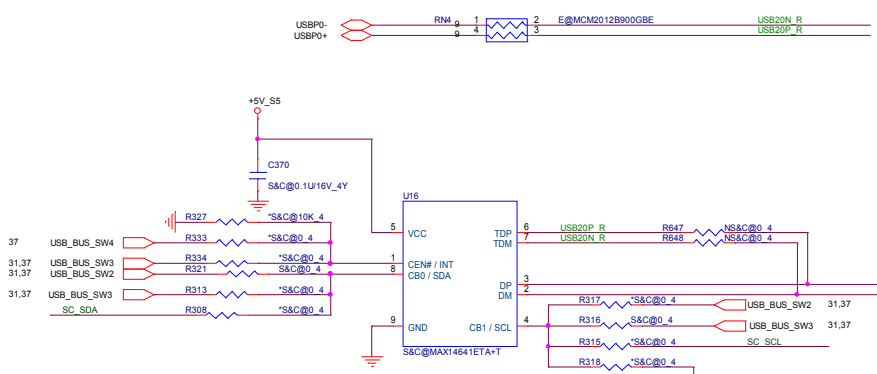
## HDMI-SMBus HDM/HMU/HMV







FOR ICT CHECK ONLY!!!



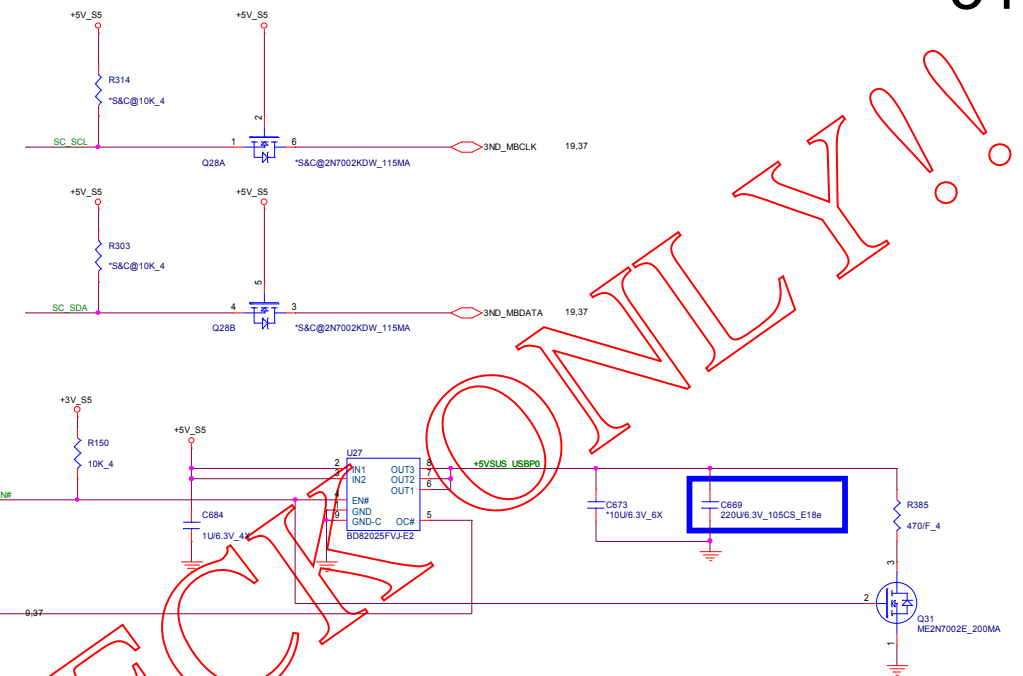
	R333	R334	R316	R318	R327	R321	R313	R308	R315
14566		V		V					
14600			V			V			
14617(with CB2)	V		V						
14617(no CB2)			V		V				
14641/14642/14644		V				V			
14640							V	V	

SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

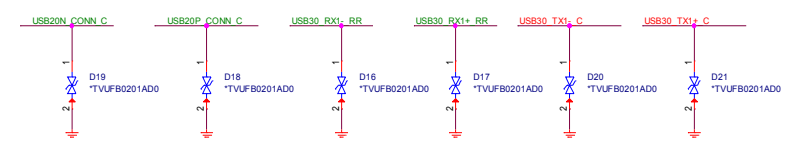
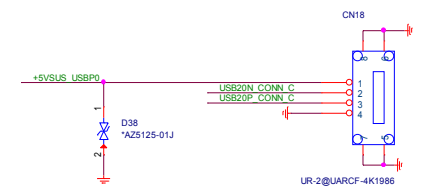
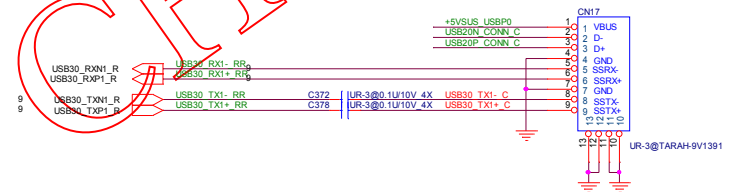
SW3	SW2	14641	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	0	Force 1A for Apple device	Charger , AP1
0	1	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW3	SW2	14644	
CB1	CB0	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	0	Force dedicated charger mode	Charger , FM
0	1	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW3	SW2	14642	
CB1	CB0	Status	
X	0	2A Auto mode for Apple device	Charger , AM2
0	1	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM



CHECK ONLY!!



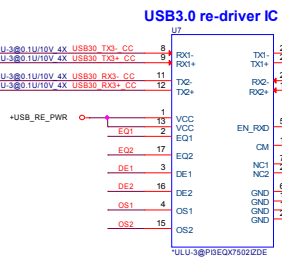
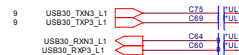
USB CONNECT  
LEFT1(ULU)

&lt;U3B/USB&gt;

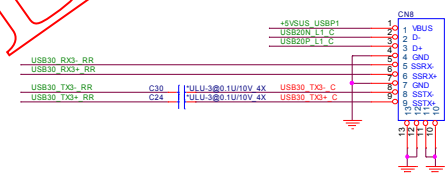
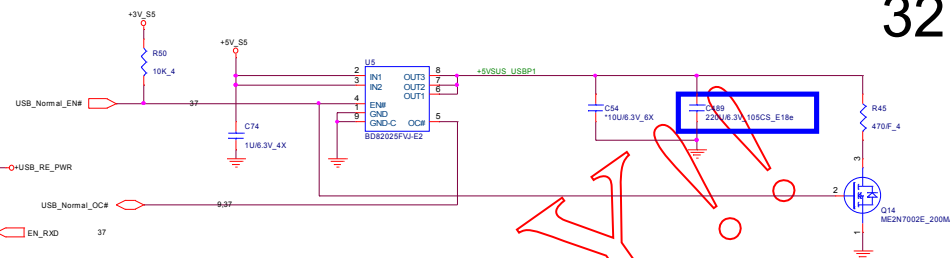
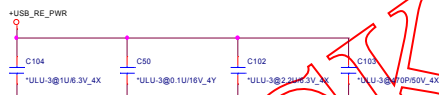
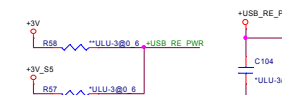
USB 3.0  
Rdriver IC

&lt;U3B&gt;

## USB3.0 re-driver IC



Control pins setting			
EN_RXD	Device function	CM	Device function
1 (default)	Normal Operation	0 (default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode



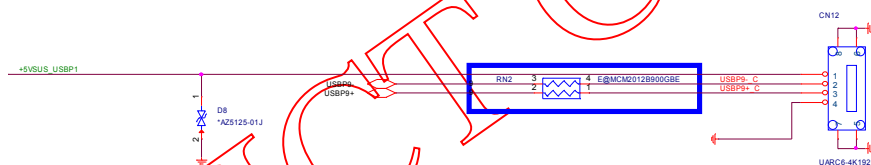
\*ULU-3@TARAB-9V1391

CN9

UARC6-4K1926

USB CONNECT  
LEFT2(ULD)

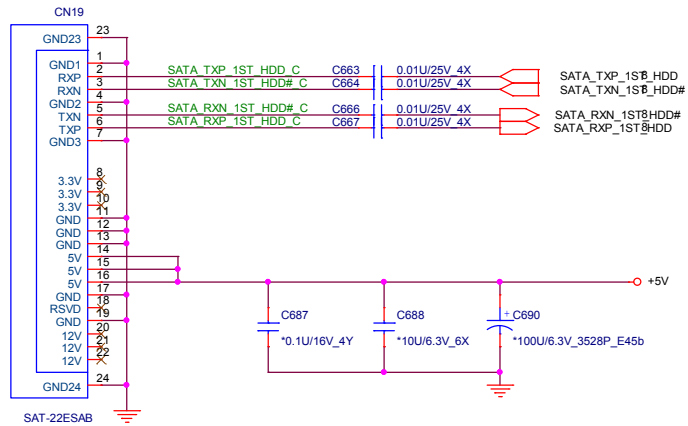
ULD



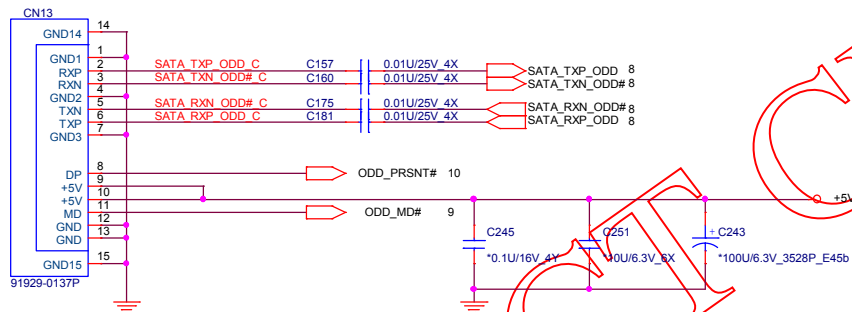


SATA  
HDD

## HDD



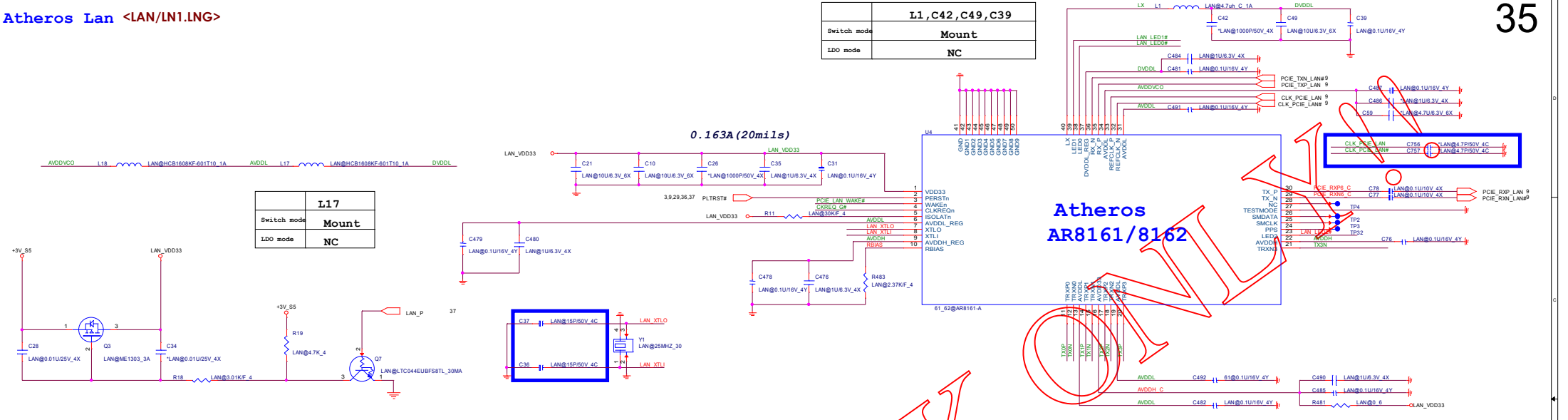
## SATA ODD &lt;ODD&gt;



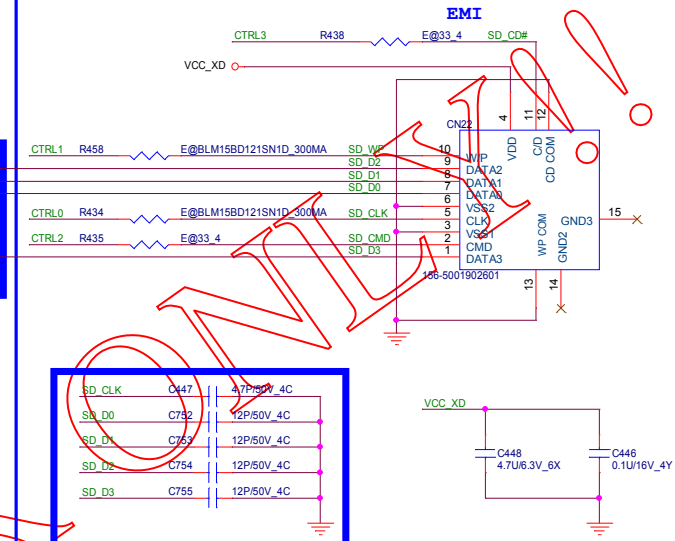
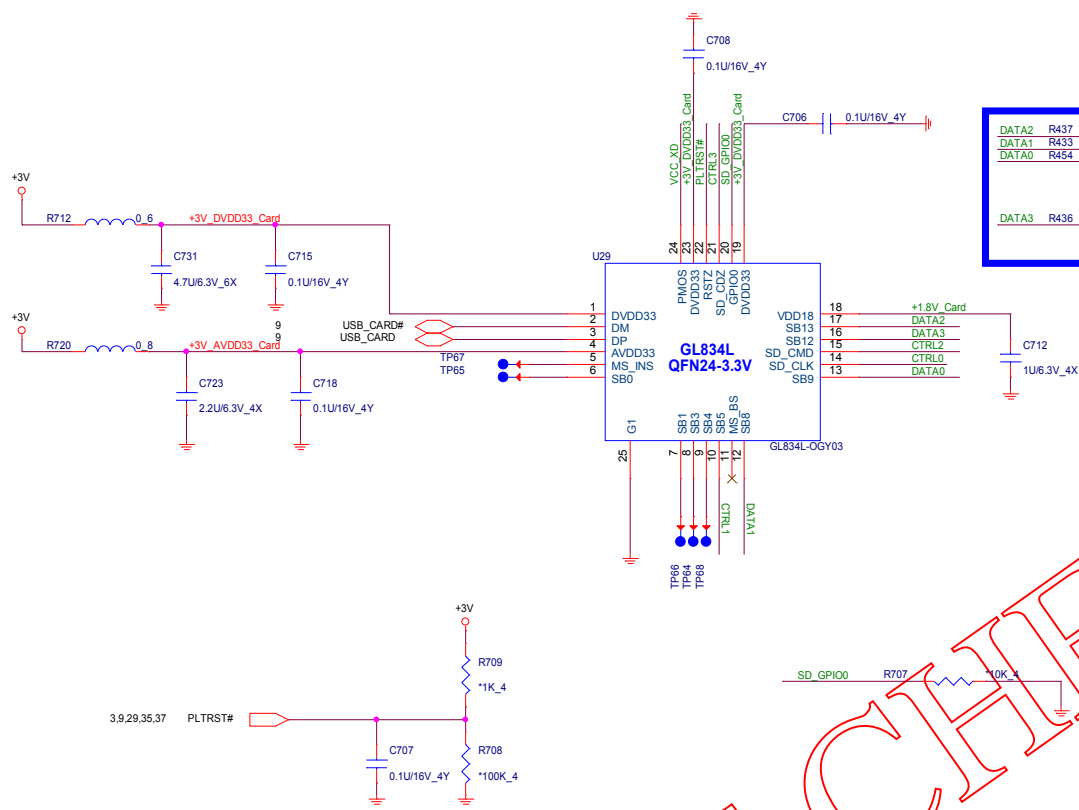
Quanta Computer Inc.

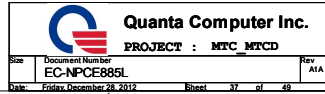
PROJECT : MTC\_MTC

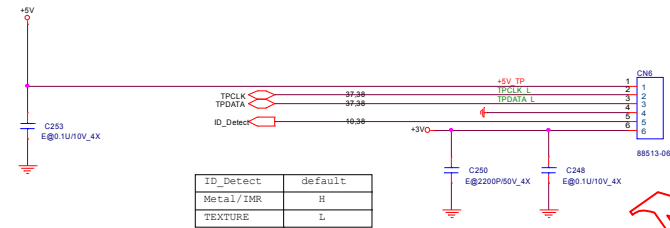
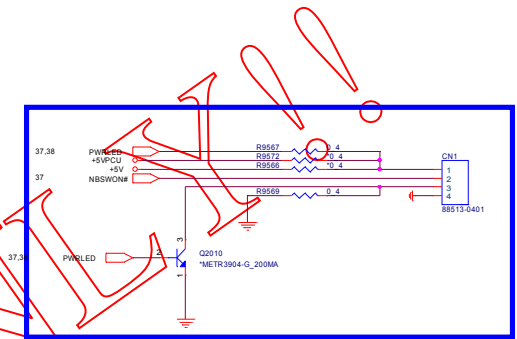




FOR INFORMATION

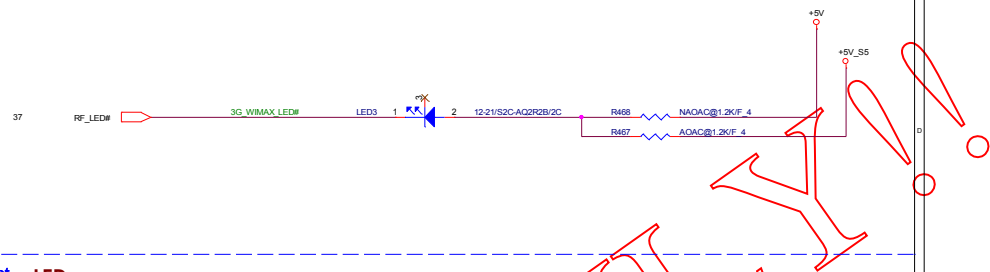
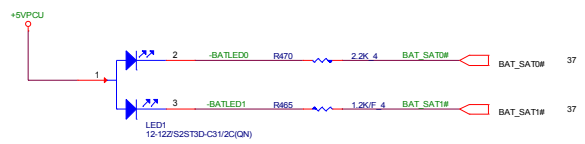






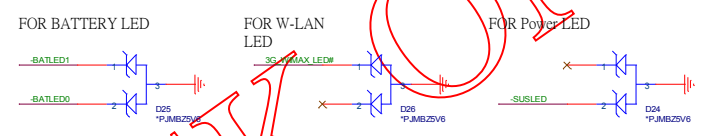
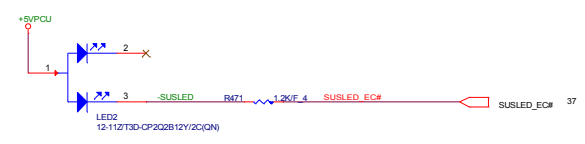
LED BATTERY

RF LED

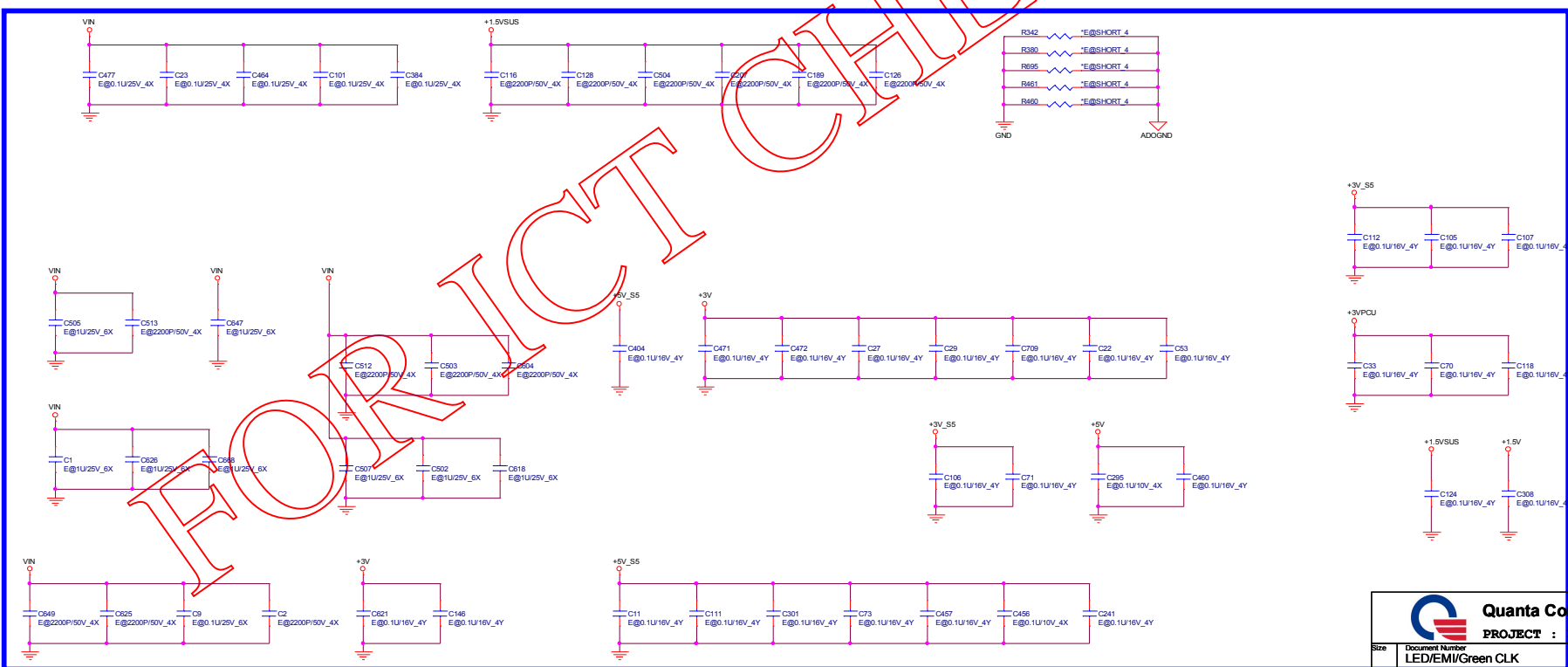


POWER LED

ESD Protect LED



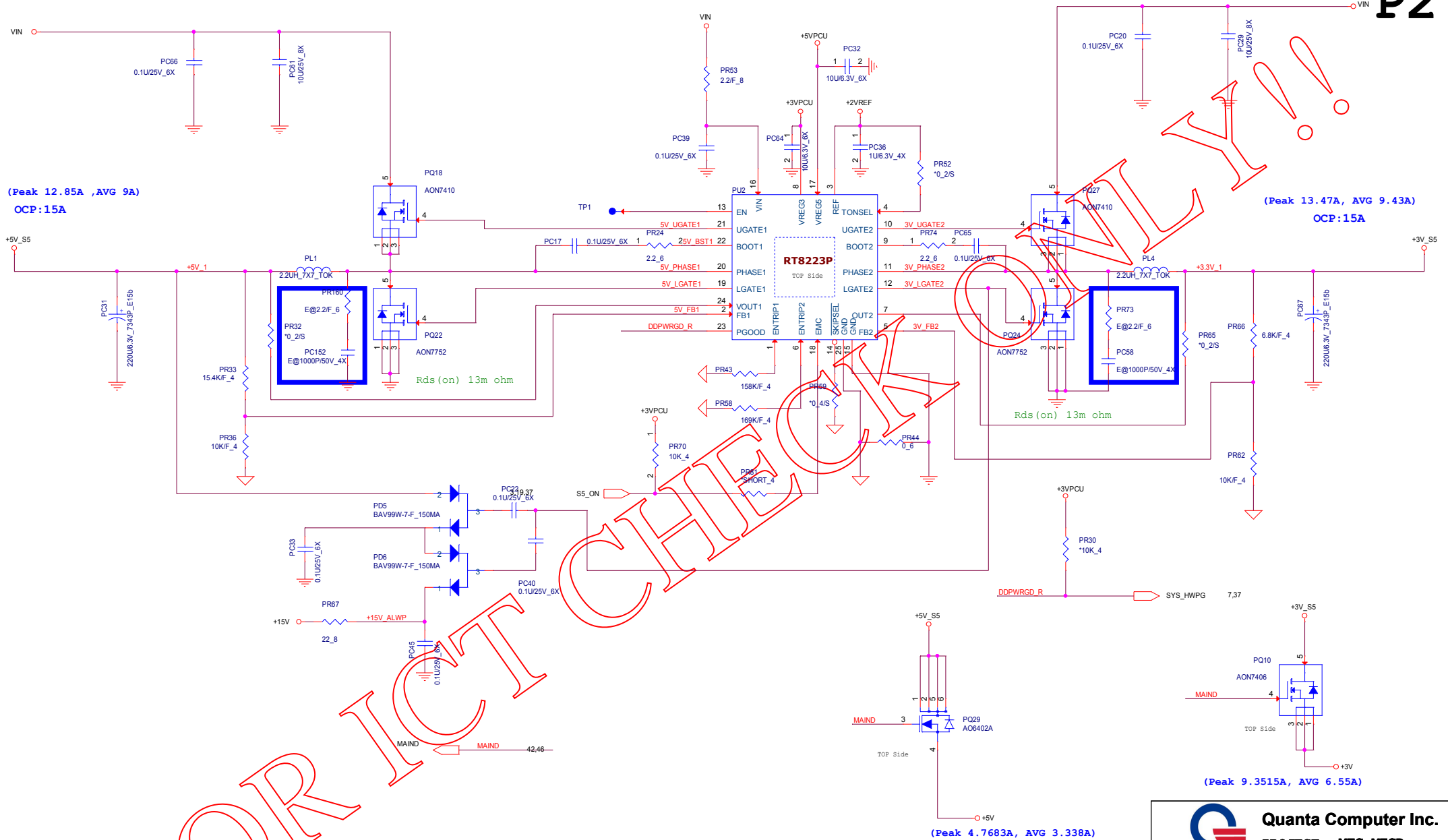
EMI







Size	Document Number	Rev
	CHARGER-ISL88731C	A1A
Date:	Friday, December 28, 2012	Sheet 40 of 49

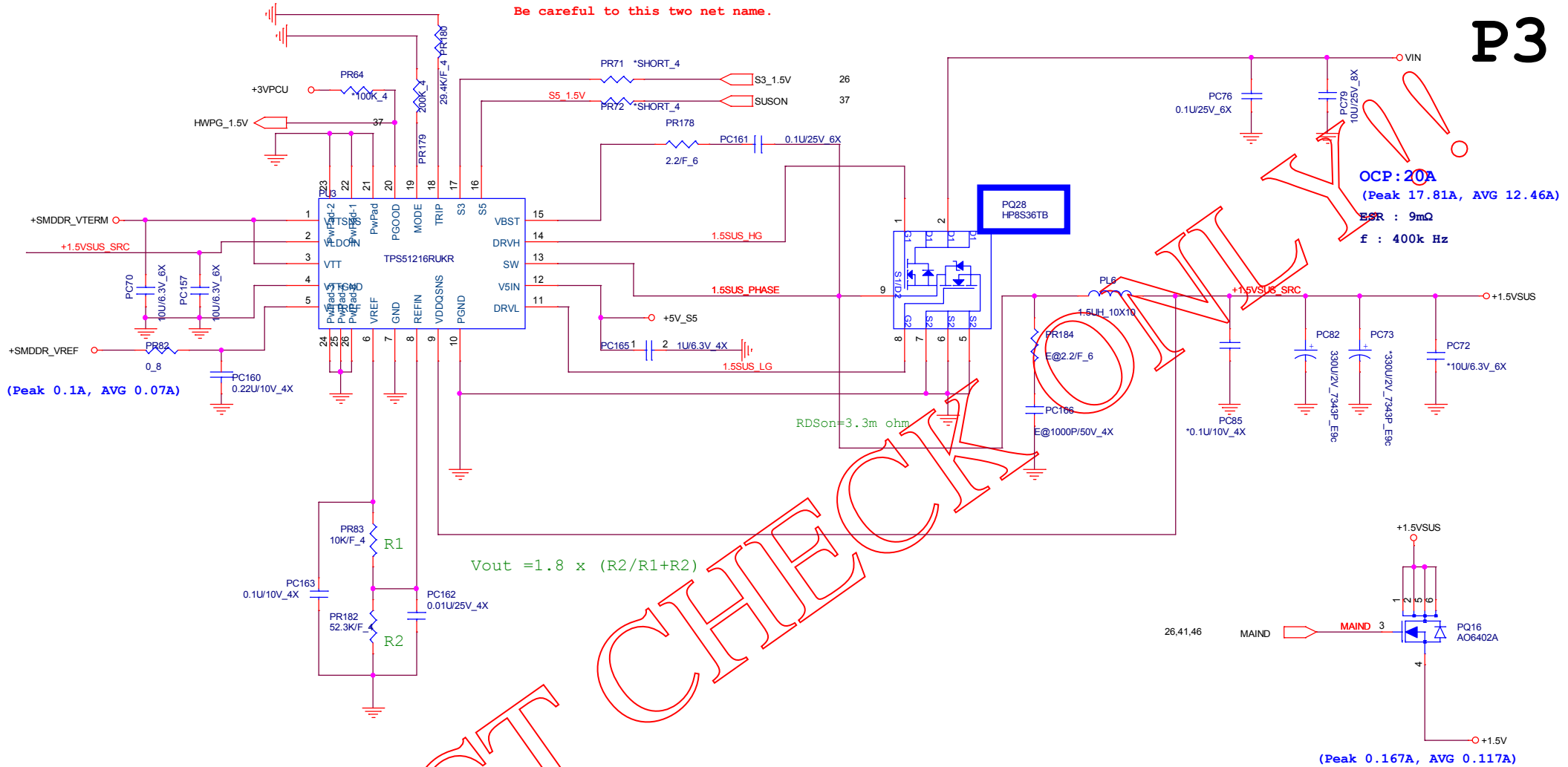


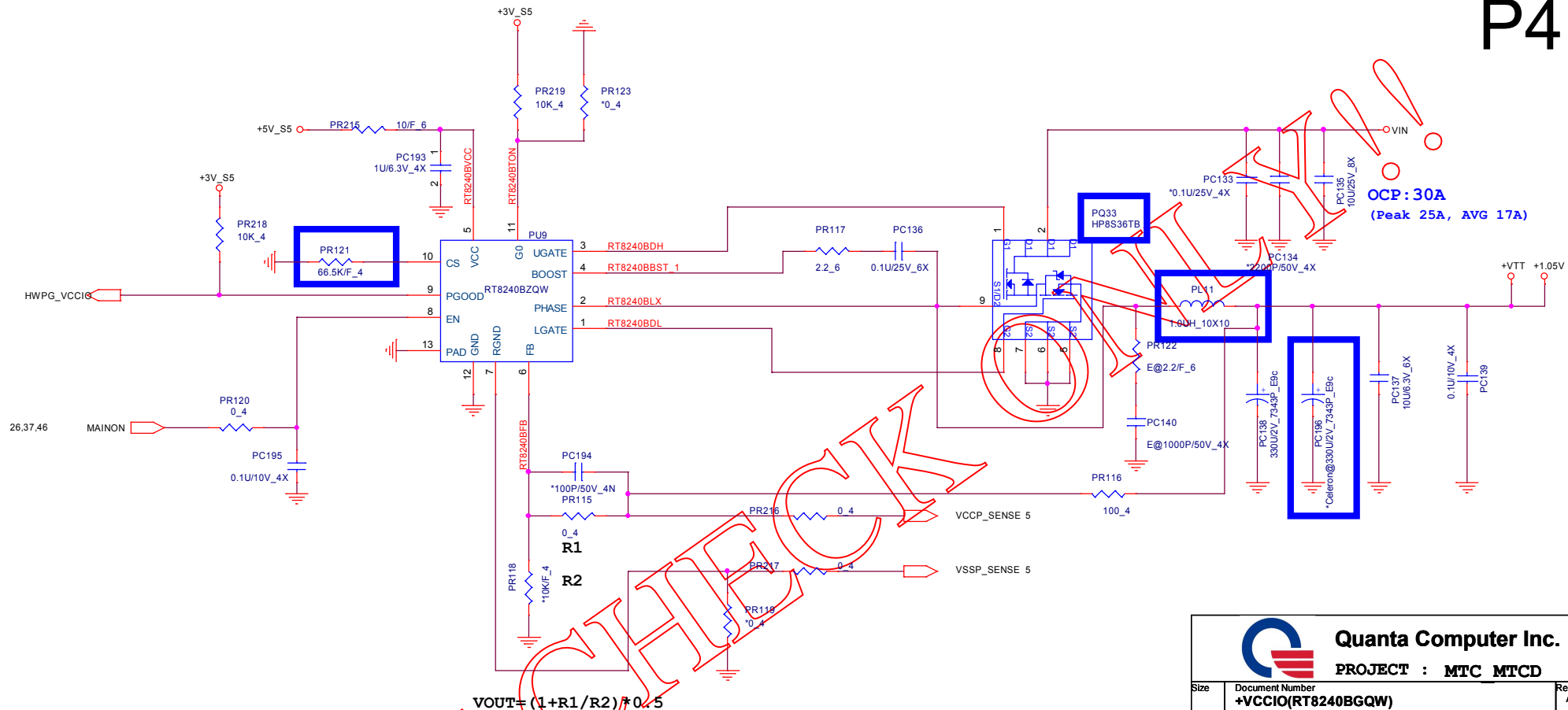
**Quanta Computer Inc.**

**PROJECT : MTC\_MTC**

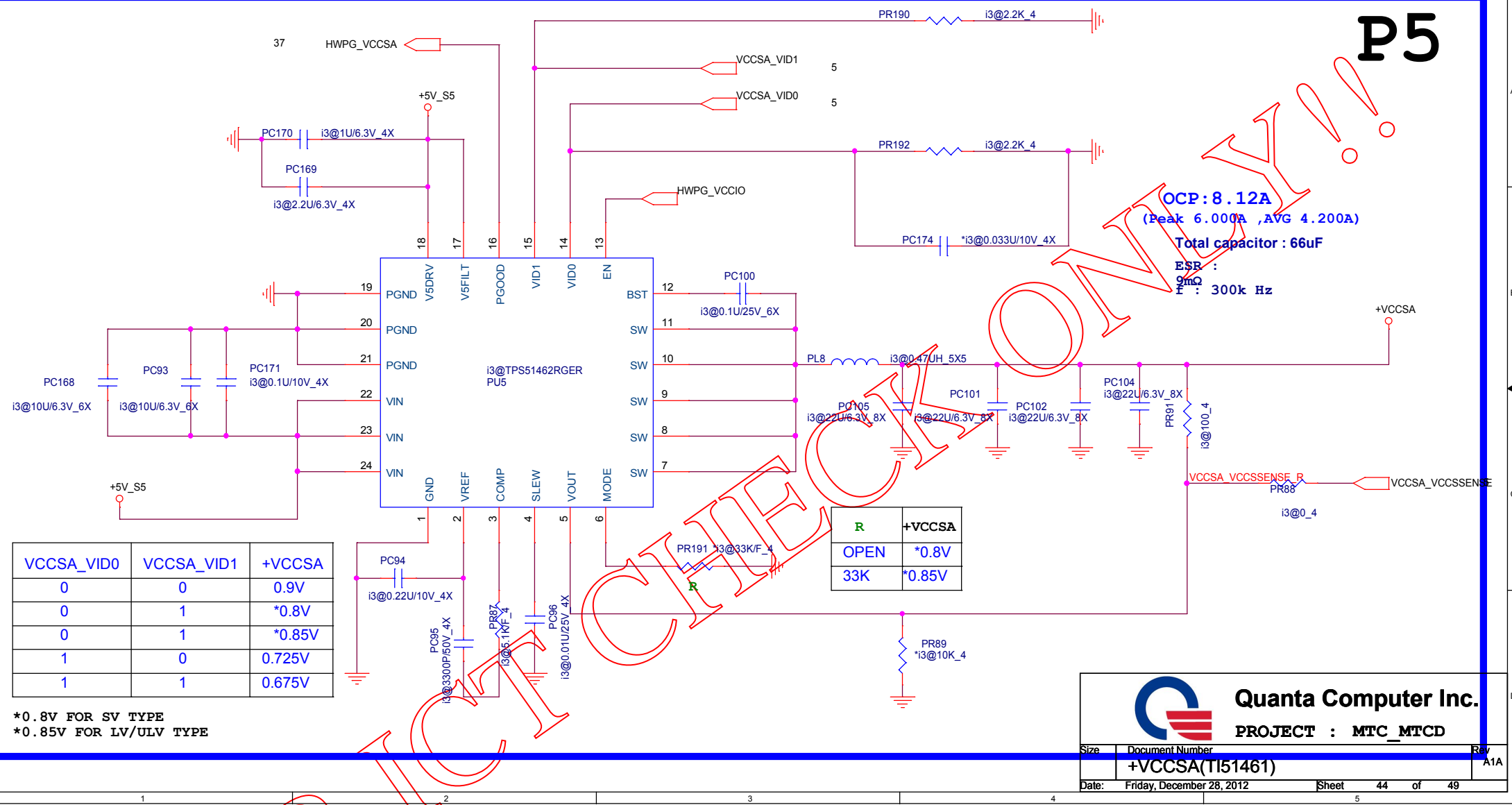
Size	Document Number	Rev
	System 3V/5V(TPS51123A)	A1A
Date:	Friday, December 28, 2012	Sheet 41 of 49

Be careful to this two net name.





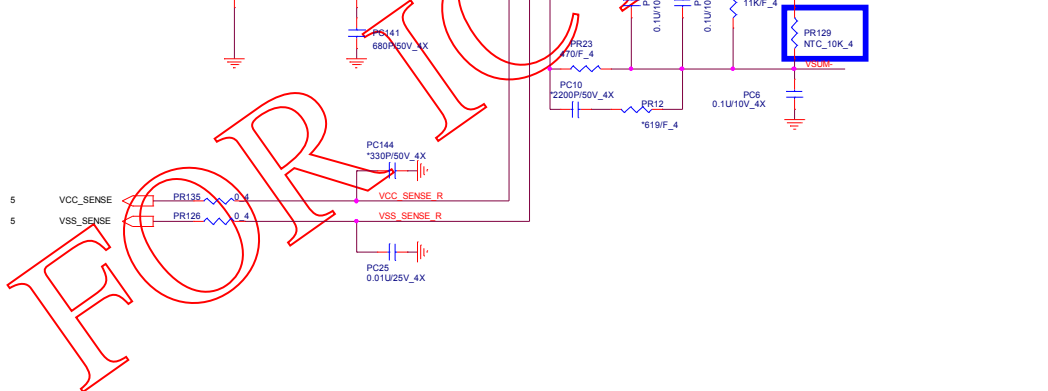
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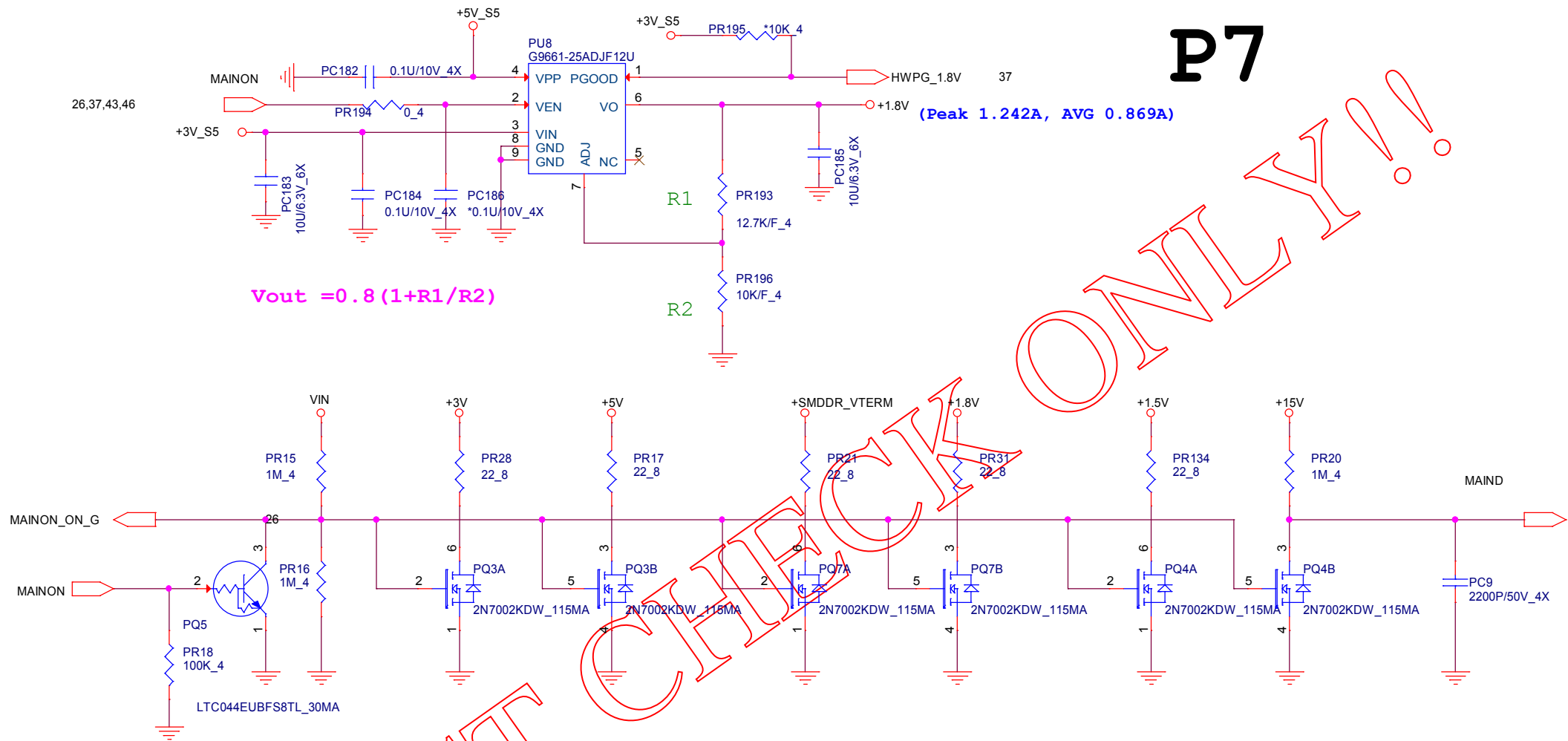
**Quanta Computer Inc.**  
**PROJECT : MTC\_MTC**

Size	Document Number	Rev
	+VCCSA(TI51461)	A1A
Date:	Friday, December 28, 2012	Sheet 44 of 49

FOR IC



P7



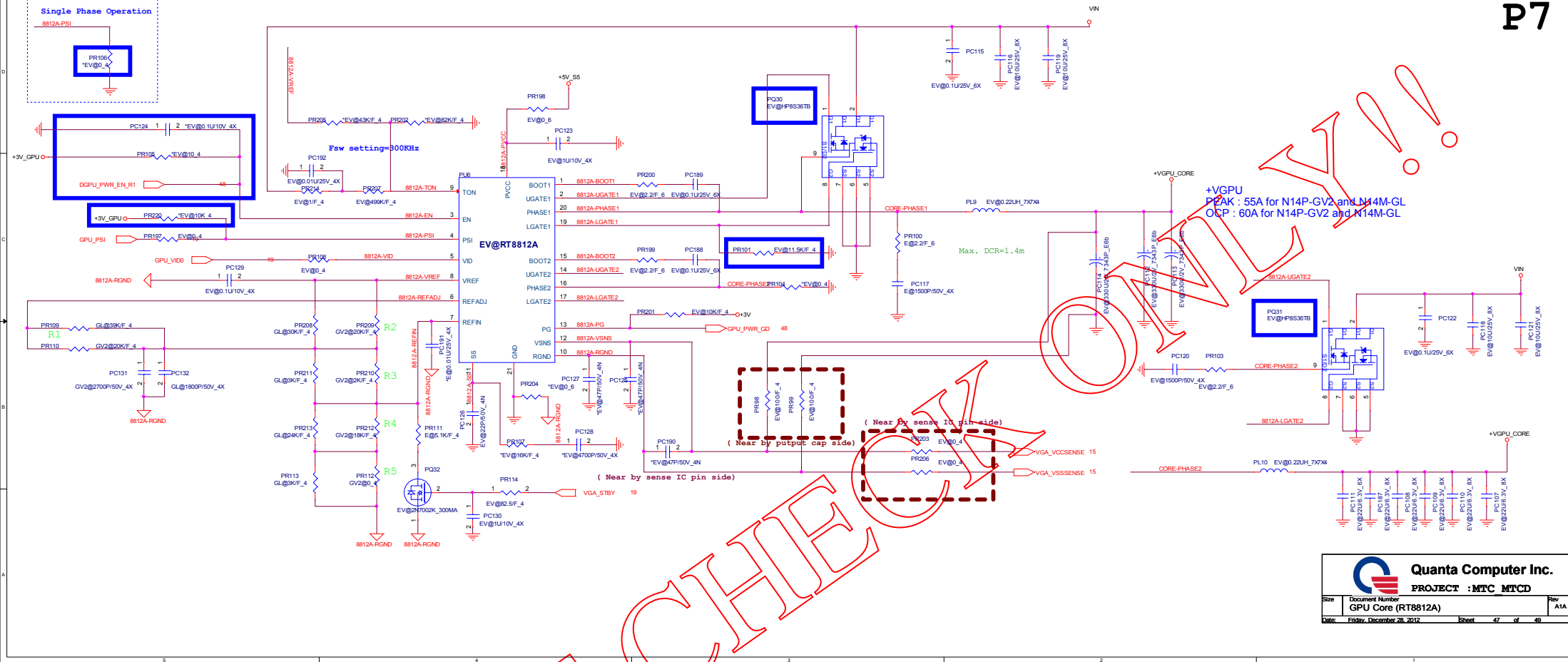
Quanta Computer Inc.

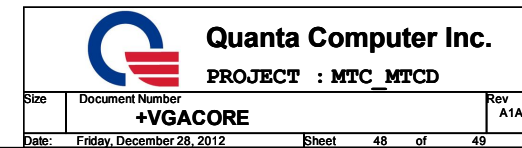
PROJECT :MTC\_MTC

Size	Document Number	Rev
	+1.8V/Discharge	A1A
Date:	Friday, December 28, 2012	Sheet 46 of 49



### Single Phase Operation





Model		REV	CHANGE LIST		MODEL		MTC/MTD	
					PAGE	FROM	To	
MTC/MTCD	A1A	Schematic Release			1	1A		
					2	1A		
					3	1A		
					4	1A		
					5	1A		
					6	1A		
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